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IIDC 1394-based Digital Camera Specification Ver.1.32

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Abstract:

The purpose of this document is to act as a design guide for digital camera makers that wish to use IEEE 1394 as the camera-to-PC interconnect. Adherences to the design specifications contained herein do not guarantee, but will promote interoperability for this class of device. The camera registers, fields within those registers, video formats, modes of operation and controls for each are specified. Area has been left for growth. To make application for additional specification, contact the 1394 Trade Association Instrumentation and Industrial Control Working Group, Digital Camera Sub Working Group (1394-TA II-WG IIDC-SWG). IIDC v1.32 is enhanced version of IIDC v1.31 with additional features and capabilities.

Keywords:

IIDC, Camera, IEEE-1394, Digital Video, Isochronous, Asynchronous

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Foreword (This foreword is not part of 1394 Trade Association Specification 2007009)

This specification defines IIDC 1394-based Digital Camera Specification for industrial use. This document describes control and status registers definition and its control procedures.

There are four annexes in this specification. Annex A is informative, Annex B is informative, Annex C is normative and Annex D is informative.

This specification was accepted by the Board of Directors of the 1394 Trade Association. Board of Directors acceptance of this specification does not necessarily imply that all board members voted for acceptance. At the time it accepted this specification, the 1394 Trade Association. Board of Directors had the following members:

Eric Anderson, Chair
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IIDC 1394-based Digital Camera Specification Ver.1.32

1 Scope and purpose

1.1 Scope

This document specifies the IIDC 1394-based Digital Camera Specification for industrial use. This document describes control and status register definitions and control procedures.

1.2 Purpose

The purpose of this specification is to describe an enhanced version of the IIDC specification for industrial cameras. This version of the specification adds new features and capabilities and is also backward compatible with earlier IIDC versions.

2 Normative references

2.1 Reference scope

The specifications and standards named in this section contain provisions, which, through reference in this text, constitute provisions of this 1394 Trade Association Specification. At the time of publication, the editions indicated were valid. All specifications and standards are subject to revision; parties to agreements based on this 1394 Trade Association Specification are encouraged to investigate the possibility of applying the most recent editions of the specifications and standards indicated below.

2.2 Approved references

The following approved specifications and standards may be obtained from the organizations that control them.

IEEE Std 1394-2008, Standard for a High Performance Serial Bus

TA2003017: IIDC 1394-based Digital Camera Specification, Version 1.31

Throughout this document, the term “IEEE 1394" shall be understood to refer to IEEE Std 1394-2008.

2.3 References under development

At the time of publication, the following referenced specifications and standards were under development.

2.4 Reference acquisition

The references cited may be obtained from the organizations that control them:

1394 Trade Association, 1560 East Southlake Blvd, Suite 220, Southlake, TX 76092 USA; (817) 416-2200 / (817) 416-2256 (FAX); http://www.1394ta.org/

American National Standards Institute (ANSI), 11 West 42nd Street, New York, NY 10036, USA; (212) 642-4900 / (212) 398-0023 (FAX); http://www.ansi.org/

Institute of Electrical and Electronic Engineers (IEEE), 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA; (732) 981-0060 / (732) 981-1721 (FAX); http://www.ieee.org/

In addition, many of the documents controlled by the above organizations may also be ordered through a third party:

Global Engineering Documents, 15 Inverness Way, Englewood, CO 80112-5776; (800) 624-3974 / (303) 792-2192; http://www.global.ihs.com/

3 Definitions and notation

3.1 Definitions

3.1.1 Conformance

Several keywords are used to differentiate levels of requirements and optionality, as follows:

3.1.1.1 expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this specification. Other hardware and software design models may also be implemented.

3.1.1.2 ignored: A keyword that describes bits, bytes, quadlets, octlets or fields whose values are not checked by the recipient.

3.1.1.3 may: A keyword that indicates flexibility of choice with no implied preference.

3.1.1.4 reserved: A keyword used to describe objects (bits, bytes, quadlets, octlets and fields) or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other specifications. A reserved object shall be zeroed or, upon development of a future specification, set to a value specified by such a specification. The recipient of a reserved object shall ignore its value. The recipient of an object defined by this specification as other than reserved shall inspect its value and reject reserved code values.

3.1.1.5 shall: A keyword that indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this specification.

3.1.1.6 should: A keyword that denotes flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “is recommended.”

3.1.2 Glossary

The following terms are used in this specification:

3.1.2.1 definition: Press ENTER to create a subsequent numbered definition paragraph …

3.1.3 Abbreviations

The following are abbreviations that are used in this specification:

XXX	The “Normal Indent” paragraph style is used for abbreviations
CSR	Control and status register [D1]

As exemplified by CSR, abbreviations may cite a bibliographic reference.

3.2 Notation

3.2.1 Numeric values

Decimal and hexadecimal are used within this specification. By editorial convention, decimal numbers are most frequently used to represent quantities or counts. Addresses are uniformly represented by hexadecimal numbers. Hexadecimal numbers are also used when the value represented has an underlying structure that is more apparent in a hexadecimal format than in a decimal format.

Decimal numbers are represented by Arabic numerals without subscripts or by their English names. Hexadecimal numbers are represented by digits from the character set 0 – 9 and A – F followed by the subscript 16. When the subscript is unnecessary to disambiguate the base of the number it may be omitted. For the sake of legibility hexadecimal numbers are separated into groups of four digits separated by spaces.

As an example, 42 and $2A_{16}$ both represent the same numeric value.

3.2.2 Bit, byte and quadlet ordering

This specification uses the facilities of Serial Bus, IEEE 1394, and therefore uses the ordering conventions of Serial Bus in the representation of data structures. In order to promote interoperability with memory buses that may have different ordering conventions, this specification defines the order and significance of bits within bytes, bytes within quadlets and quadlets within octlets in terms of their relative position and not their physically addressed position.

For legacy reasons, this IIDC specification uses a bit ordering convention that is opposite the standard convention. Within a byte, the most significant bit, *msb*, is that which is transmitted last and the least significant bit, *lsb*, is that which is transmitted first on Serial Bus, as illustrated below. The significance of the interior bits uniformly decreases in progression from *lsb* to *msb*.

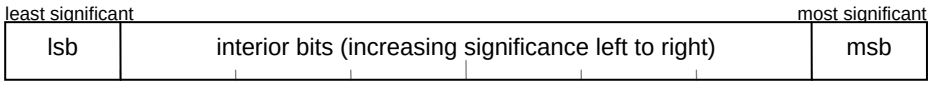


Figure 1 – Bit ordering within a byte

Within a quadlet, the most significant byte is that which is transmitted first and the least significant byte is that which is transmitted last on Serial Bus, as shown below.

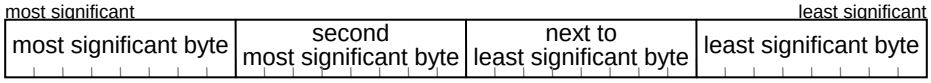


Figure 2 – Byte ordering within a quadlet

Within an octlet, which is frequently used to contain 64-bit Serial Bus addresses, the most significant quadlet is that which is transmitted first and the least significant quadlet is that which is transmitted last on Serial Bus, as the figure below indicates.

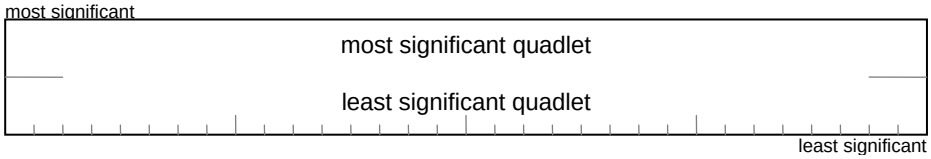


Figure 3 – Quadlet ordering within an octlet

When block transfers take place that are not quadlet aligned or not an integral number of quadlets, no assumptions can be made about the ordering (significance within a quadlet) of bytes at the unaligned beginning or fractional quadlet end of such a block transfer, unless an application has knowledge (outside of the scope of this specification) of the ordering conventions of the other bus.

3.2.3 Register specifications

This specification defines the format and function of control and status registers, CSRs. Some of these registers are read-only, some are both readable and writable and some generate special side effects subsequent to a write.

In order to define CSRs, their bit fields, their initial values and the effects of read, write or other transactions, the format illustrated by Figure 4 is used.

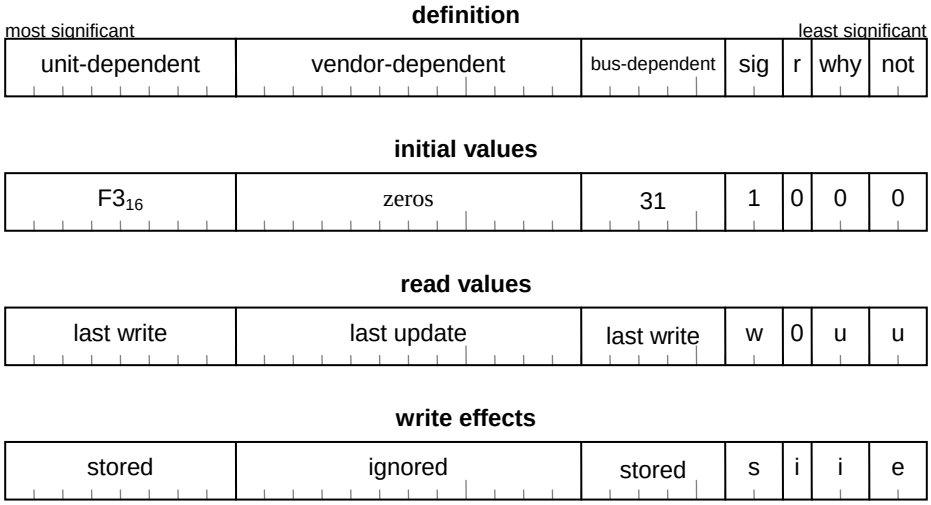


Figure 4 – CSR specification example

The register definition contains the names of register fields. The names are intended to be descriptive, but the fields are defined in the text; their function should not be inferred solely from their names. However, the following field names have defined meanings.

Name	Abbreviation	Definition
bus-dependent		The meaning of the field is defined by the bus standard, in this case IEEE 1394
reserved	r	The field is reserved for future standardization (see 3.1.1)
unit-dependent		The meaning of the field shall be defined by the organization responsible for the unit architecture
vendor-dependent		The meaning of the field shall be defined by the node's vendor

CSRs shall assume initial values upon the restoration of power (a power reset) or upon a write to the node's RESET_START register (a command reset). If the power reset values differ from the command reset values, they are separately and explicitly defined. Initial values for register fields may be described as numeric constants or with one of the terms defined for the register definition. Values for register fields subsequent to a reset may be described in the same terms or as defined below.

Name	Abbreviation	Definition
unchanged	x	The field retains whatever value it had just prior to the power reset, bus reset or command reset.

In addition to numeric values for constant fields, the read values returned in response to a quadlet read transaction may be specified by the terms below.

Name	Abbreviation	Definition
last write	w	The value of the field shall be either the initial value or, if a write or lock transaction addressed to the register has successfully completed, the value most recently stored in the field.[1]
last update	u	The value of the field shall be that most recently updated by the node hardware or software. An updated field value may be the result of a write effect to the same register address, a different register address or some other change of condition within the node.

The effects of data written to the register are specified by the terms below.

Name	Abbreviation	Definition
effect	e	The value of the data written to the field may have an effect on the node's state, but the effect might not be immediately visible by a read of the same register. The effect may be visible in another register or might not be visible at all.
ignored	i	The value of the data written to the field shall be ignored; it shall have no effect on the node's state.
stored	s	The value of the data written to the field shall be immediately visible by a read of the same register; it may also have other effects on the node's state.

Reserved fields within a register shall be explicitly described with respect to initial values, read values and write effects. Initial values and read values shall be zero while write effects shall be ignored. CSRs that are not implemented, either because they are optional or they fall within a reserved address space, shall abide by these same conventions if a successful completion response is returned for a read, write or lock request.

[1] For clarity, read values for a field in a register that accepts lock transactions may be described as *last successful lock* rather than *last write*. However, the abbreviation in both cases remains *w*. Similar liberties may be taken with the use of *conditionally stored* in place of *stored* when the action occurs as the result of a lock transaction, but the corresponding one-letter abbreviation, *s*, is also unchanged.

4 Digital camera control command register

Base address for all digital camera command registers is:

Bus_ID, Node_ID , FFFF Fxxx xxxx (initial units space)

This address is contained in the configuration ROM in the camera unit directory.

The following sections define the entire camera CSR registers. The offset field in each of the tables is the byte offset from the above base address.

4.1 Camera initialize register

Offset	Name	Field	Bit	Description
000h	INITIALIZE	Initialize	[0]	If you assert this bit, Camera will re-set to initial state. This bit is self cleared, shall wait becoming “0”
		-	[1..31]	Reserved

	0-7	8-15	16-23	24-31
i	Reserved			

Initial values	System dependent
Read values	‘0’ Done ‘1’ Busy (under initialization)
Write effect	'0' no effect '1' set initial state

4.2 Inquiry register for video format/mode/frame rate

Each bit in the inquiry fields specifies the availability of a given feature. A value of '1' indicates that the corresponding feature is implemented; a value of '0' indicates that the corresponding feature is not implemented. The following sections define the inquiry registers.

4.2.1 Inquiry register for video format

Offset	Name	Field	Bit	Description
100h	V_FORMAT_INQ	Format_0	[0]	VGA non-compressed format. (Maximum 640x480)
		Format_1	[1]	Super VGA non-compressed format (1)
		Format_2	[2]	Super VGA non-compressed format (2)
		Format_x	[3..5]	Reserved for other format.
		Format_6	[6]	Still Image Format
		Format_7	[7]	Partial Image Size Format
		-	[8..31]	Reserved

0-7	8-15	16-23	24-31
Format	Reserved		

Initial values	System dependent.
Read values	System dependent. Same value to Initial value.
Write effect	Ignored.

4.2.2 Inquiry register for video mode

Offset	Name	Field	Bit	Description
180h	V_MODE_INQ_0 (Format_0)	Mode_0	[0]	160 X 120 YUV(4:4:4) Mode (24bit/pixel)
		Mode_1	[1]	320 X 240 YUV(4:2:2) Mode (16bit/pixel)
		Mode_2	[2]	640 X 480 YUV(4:1:1) Mode (12bit/pixel)
		Mode_3	[3]	640 X 480 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	640 X 480 RGB Mode (24bit/pixel)
		Mode_5	[5]	640 X 480 Y (Mono) Mode (8bit/pixel)
		Mode_6	[6]	640 X 480 Y (Mono16) Mode (16bit/pixel)
		Mode_x	[7]	Reserved for another Mode
		-	[8..31]	Reserved
184h	V_MODE_INQ_1 (Format_1)	Mode_0	[0]	800 X 600 YUV(4:2:2) Mode (16bit/pixel)
		Mode_1	[1]	800 X 600 RGB Mode (24bit/pixel)
		Mode_2	[2]	800 X 600 Y (Mono) Mode (8bit/pixel)
		Mode_3	[3]	1024 X 768 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	1024 X 768 RGB Mode (24bit/pixel)
		Mode_5	[5]	1024 X 768 Y (Mono) Mode (8bit/pixel)
		Mode_6	[6]	800 X 600 Y (Mono16) Mode (16bit/pixel)
		Mode_7	[7]	1024 X 768 Y (Mono16) Mode (16bit/pixel)
		-	[8..31]	Reserved
188h	V_MODE_INQ_2 (Format_2)	Mode_0	[0]	1280 X 960 YUV(4:2:2) Mode (16bit/pixel)
		Mode_1	[1]	1280 X 960 RGB Mode (24bit/pixel)
		Mode_2	[2]	1280 X 960 Y (Mono) Mode (8bit/pixel)
		Mode_3	[3]	1600 X 1200 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	1600 X 1200 RGB Mode (24bit/pixel)
		Mode_5	[5]	1600 X 1200 Y (Mono) Mode (8bit/pixel)
		Mode_6	[6]	1280 X 960 Y (Mono16) Mode (16bit/pixel)
		Mode_7	[7]	1600X 1200 Y (Mono16) Mode (16bit/pixel)
		-	[8..31]	Reserved
18Ch : 197h	Reserved for other V_MODE_INQ_x for Format_x.			
198h	V_MODE_INQ_6 (Format_6)	Mode_0	[0]	Exif format
		Mode_x	[1..7]	Reserved for another Mode
		-	[8..31]	Reserved
19Ch	V_MODE_INQ_7 (Format_7)	Mode_0	[0]	Format_7_Mode_0
		Mode_1	[1]	Format_7 Mode_1
		Mode_2	[2]	Format_7 Mode_2
		Mode_3	[3]	Format_7 Mode_3
		Mode_4	[4]	Format_7 Mode_4
		Mode_5	[5]	Format_7 Mode_5
		Mode_6	[6]	Format_7 Mode_6
		Mode_7	[7]	Format_7 Mode_7
		Mode_8	[8]	Format_7 Mode_8
		Mode_9	[9]	Format_7 Mode_9
		Mode_10	[10]	Format_7 Mode_10
		Mode_11	[11]	Format_7 Mode_11
		Mode_12	[12]	Format_7 Mode_12
		Mode_13	[13]	Format_7 Mode_13
		Mode_14	[14]	Format_7 Mode_14
		Mode_15	[15]	Format_7 Mode_15
		Mode_16	[16]	Format_7 Mode_16
		Mode_17	[17]	Format_7 Mode_17
		Mode_18	[18]	Format_7 Mode_18
		Mode_19	[19]	Format_7 Mode_19

		Mode_20	[20]	Format_7 Mode_20
		Mode_21	[21]	Format_7 Mode_21
		Mode_22	[22]	Format_7 Mode_22
		Mode_23	[23]	Format_7 Mode_23
		Mode_24	[24]	Format_7 Mode_24
		Mode_25	[25]	Format_7 Mode_25
		Mode_26	[26]	Format_7 Mode_26
		Mode_27	[27]	Format_7 Mode_27
		Mode_28	[28]	Format_7 Mode_28
		Mode_29	[29]	Format_7 Mode_29
		Mode_30	[30]	Format_7 Mode_30
		Mode_31	[31]	Format_7 Mode_31

0-7	8-15	16-23	24-31
V_MODE_INQ			

Initial values	System dependent
Read values	System dependent. Same value to Initial value
Write effect	Ignored

4.2.3 Inquiry register for video frame rate and base address of the Video Mode CSR for the Partial Image Size Format

Offset	Name	Field	Bit	Description
200h	V_RATE_INQ_0_0 (Format_0,Mode_0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
204h	V_RATE_INQ_0_1 (Format_0,Mode_1)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
208h	V_RATE_INQ_0_2 (Format_0,Mode_2)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
20Ch	V_RATE_INQ_0_3 (Format_0,Mode_3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
210h	V_RATE_INQ_0_4 (Format_0,Mode_4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
214h	V_RATE_INQ_0_5 (Format_0,Mode_5)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps

		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
218h	V_RATE_INQ_0_6 (Format_0,Mode_6)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
21Ch : 21Fh	Reserved V_RATE_INQ_0_x (for other Mode_x of Format_0)			
220h	V_RATE_INQ_1_0 (Format_1,Mode_0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
224h	V_RATE_INQ_1_1 (Format_1,Mode_1)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
228h	V_RATE_INQ_1_2 (Format_1,Mode_2)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
22Ch	V_RATE_INQ_1_3 (Format_1,Mode_3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps

		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
230h	V_RATE_INQ_1_4 (Format_1,Mode_4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
234h	V_RATE_INQ_1_5 (Format_1,Mode_5)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
238h	V_RATE_INQ_1_6 (Format_1,Mode_6)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
		-	[8..31]	Reserved
23Ch	V_RATE_INQ_1_7 (Format_1,Mode_7)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
240h	V_RATE_INQ_2_0 (Format_2,Mode_0)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
244h	V_RATE_INQ_2_1 (Format_2,Mode_1)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps

		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
248h	V_RATE_INQ_2_2 (Format_2,Mode_2)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
24Ch	V_RATE_INQ_2_3 (Format_2,Mode_3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
250h	V_RATE_INQ_2_4 (Format_2,Mode_4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	Reserved
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
254h	V_RATE_INQ_2_5 (Format_2,Mode_5)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
258h	V_RATE_INQ_2_6 (Format_2,Mode_6)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
25Ch	V_RATE_INQ_2_7 (Format_2,Mode_7)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps

		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
		-	[8..31]	Reserved
260h : 2BFh	Reserved V_RATE_INQ_y_x (for other Format_y,Mode_x)			
2C0h	V_REV_INQ_6_0 (Format_6,Mode_0)	revision_0	[0]	Exif format revision 2.0
		revision_x	[1..7]	Reserved for other revision
		-	[8..31]	Reserved
2C4h : 2DFh	Reserved V_REV_INQ_6_x (for other Mode_x of Format_6)			
2E0h	V_CSR_INQ_7_0	Mode_0	[0..31]	CSR quadlet offset for Format_7 Mode_0
2E4h	V_CSR_INQ_7_1	Mode_1	[0..31]	CSR quadlet offset for Format_7 Mode_1
2E8h	V_CSR_INQ_7_2	Mode_2	[0..31]	CSR quadlet offset for Format_7 Mode_2
2ECh	V_CSR_INQ_7_3	Mode_3	[0..31]	CSR quadlet offset for Format_7 Mode_3
2F0h	V_CSR_INQ_7_4	Mode_4	[0..31]	CSR quadlet offset for Format_7 Mode_4
2F4h	V_CSR_INQ_7_5	Mode_5	[0..31]	CSR quadlet offset for Format_7 Mode_5
2F8h	V_CSR_INQ_7_6	Mode_6	[0..31]	CSR quadlet offset for Format_7 Mode_6
2FCh	V_CSR_INQ_7_7	Mode_7	[0..31]	CSR quadlet offset for Format_7 Mode_7
300h	V_CSR_INQ_7_8	Mode_8	[0..31]	CSR quadlet offset for Format_7 Mode_8
304h	V_CSR_INQ_7_9	Mode_9	[0..31]	CSR quadlet offset for Format_7 Mode_9
308h	V_CSR_INQ_7_10	Mode_10	[0..31]	CSR quadlet offset for Format_7 Mode_10
30Ch	V_CSR_INQ_7_11	Mode_11	[0..31]	CSR quadlet offset for Format_7 Mode_11
310h	V_CSR_INQ_7_12	Mode_12	[0..31]	CSR quadlet offset for Format_7 Mode_12
314h	V_CSR_INQ_7_13	Mode_13	[0..31]	CSR quadlet offset for Format_7 Mode_13
318h	V_CSR_INQ_7_14	Mode_14	[0..31]	CSR quadlet offset for Format_7 Mode_14
31Ch	V_CSR_INQ_7_15	Mode_15	[0..31]	CSR quadlet offset for Format_7 Mode_15
320h	V_CSR_INQ_7_16	Mode_16	[0..31]	CSR quadlet offset for Format_7 Mode_16
324h	V_CSR_INQ_7_17	Mode_17	[0..31]	CSR quadlet offset for Format_7 Mode_17
328h	V_CSR_INQ_7_18	Mode_18	[0..31]	CSR quadlet offset for Format_7 Mode_18
32Ch	V_CSR_INQ_7_19	Mode_19	[0..31]	CSR quadlet offset for Format_7 Mode_19
330h	V_CSR_INQ_7_20	Mode_20	[0..31]	CSR quadlet offset for Format_7 Mode_20
334h	V_CSR_INQ_7_21	Mode_21	[0..31]	CSR quadlet offset for Format_7 Mode_21
338h	V_CSR_INQ_7_22	Mode_22	[0..31]	CSR quadlet offset for Format_7 Mode_22
33Ch	V_CSR_INQ_7_23	Mode_23	[0..31]	CSR quadlet offset for Format_7 Mode_23
340h	V_CSR_INQ_7_24	Mode_24	[0..31]	CSR quadlet offset for Format_7 Mode_24
344h	V_CSR_INQ_7_25	Mode_25	[0..31]	CSR quadlet offset for Format_7 Mode_25
348h	V_CSR_INQ_7_26	Mode_26	[0..31]	CSR quadlet offset for Format_7 Mode_26
34Ch	V_CSR_INQ_7_27	Mode_27	[0..31]	CSR quadlet offset for Format_7 Mode_27
350h	V_CSR_INQ_7_28	Mode_28	[0..31]	CSR quadlet offset for Format_7 Mode_28
354h	V_CSR_INQ_7_29	Mode_29	[0..31]	CSR quadlet offset for Format_7 Mode_29
358h	V_CSR_INQ_7_30	Mode_30	[0..31]	CSR quadlet offset for Format_7 Mode_30
35Ch	V_CSR_INQ_7_31	Mode_31	[0..31]	CSR quadlet offset for Format_7 Mode_31

For Format_0, Format_1, Format_2:

0-7	8-15	16-23	24-31

FrameRate	Reserved

For Format_6:

0-7	8-15	16-23	24-31
Revision	Reserved		

For Format_7 (Partial Image Size Format):

0-7	8-15	16-23	24-31
Base address of the Video Mode CSR (quadlet offset)			

"Base address of the Video Mode CSR" is the quadlet offset from the base address of initial register space.

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.3 Inquiry register for basic function

The entire field except "Memory_Channel" is bit assignment for inquiry.

(0:Not available 1:Available)

Offset	Name	Field	Bit	Description
400h	BASIC_FUNC_INQ	Advanced_Feature_ Inq	[0]	Inquiry for advanced feature. (Vendor Unique Features)
		Vmode_Error_Status _Inq	[1]	Inquiry for existence of Vmode_Error_Status register
		Feature_Control_Error _Status_Inq	[2]	Inquiry for existence of Feature_Control_Error_Status register
		Opt_Func_CSR_Inq	[3]	Inquiry for optional function CSR.
		Ext_Format_7_Inq	[4]	Inquiry for extended Format_7 mode capability
		-	[5..7]	Reserved
		1394.b_mode _Capability	[8]	Inquiry for 1394.b mode capability
		Little_Endian_Inq	[9]	Inquiry for little endian mode support for 16bit pixel formats
		-	[10..15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/OFF capability
		-	[17..18]	Reserved
		One_Shot_Inq	[19]	One shot transmission capability
		Multi_Shot_Inq	[20]	Multi shot transmission capability
		Retransmit_Inq	[21]	Retransmit latest image capability (One_shot/Retransmit)
		Image_Buffer _Inq	[22]	Image buffer capability (Multi_shot/Image_Buffer)
		-	[23..27]	Reserved
		Memory_Channel	[28..31]	Maximum memory channel number (N) Memory channel no 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N= Memory Ch N If 0000, user memory is not available.

0-7						8-15			16-23							24-31	
a	v	f	o	e	Reserv	b	l	Reserved	c	R	o	m	r	b	R	Reserved	mem

"Advanced Feature" is vendor unique features. Vendor shall prepare CSR's for these additional features and write base address of these CSR's at 480h as a quadlet offset value from the base address of initial register space.

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.4 Inquiry register for feature presence

The following registers show presence of the camera features or optional functions. Each bit corresponds to a feature or the function. The camera, which supports multiple video formats and modes, might change the presence of a feature as reported in the following registers.

The presence bits in the following registers shall have the same values as presence bits for the same feature in other registers (5xxh, 8xxh), at all times.

The entire field is a bit assignment for inquiry. (0:Not available 1:Available)

Offset	Name	Field	Bit	Description
404h	Feature_Hi_Inq	Brightness	[0]	Brightness Control
		Auto Exposure	[1]	Auto Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Speed Control
		Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13]	Trigger Delay Control
		White_Shading	[14]	White Shading Compensation Control
		Frame_Rate	[15]	Frame rate prioritize control
		-	[16..31]	Reserved
408h	Feature_Lo_Inq	Zoom	[0]	Zoom Control
		Pan	[1]	PAN Control
		Tilt	[2]	TILT Control
		Optical Filter	[3]	Optical Filter Control
			[4..15]	Reserved
		Capture_Size	[16]	Capture image size for Format_6
		Capture_Quality	[17]	Capture image quality for Format_6
		-	[18..31]	Reserved
40Ch	Opt_Function_Inq	-	[0]	Reserved
		PIO	[1]	Parallel input/output control
		SIO	[2]	Serial Input/output control
		Strobe_Output	[3]	Strobe signal output
		Lookup_Table	[4]	Lookup table control
		-	[5..31]	Reserved
410h : 47Fh	Reserved			
480h	Advanced_Feature_ Inq	Advanced_Feature _Quadlet_Offset	[0 .. 31]	Quadlet offset of the advanced feature CSR's from the base address of initial register space. (Vendor unique)
484h	PIO_Control_CSR_Inq	PIO_Control_Quad let_Offset	[0 .. 31]	Quadlet offset of the PIO control CSR's from the base address of initial register

				space.
488h	SIO_Control_CSR_Inq	SIO_Control_Quadlet_Offset	[0 .. 31]	Quadlet offset of the SIO control CSR's from the base address of initial register space.
48Ch	Strobe_output_CSR_Inq	Strobe_Output_Quadlet_Offset	[0 .. 31]	Quadlet offset of the Strobe output signal CSR's from the base address of initial register space.
490h	Lookup_Table_CSR_Inq	Lookup_Table_Quadlet_Offset	[0 .. 31]	Quadlet offset of the Lookup Tablel CSR's from the base address of initial register space.
494h : 4FFh				Reserved for future optional functions.

offset	0-7	8-15	16-23	24-31
404h	b e s w h s g s	g l f t t t w f	Reserved	
408h	z p t o	Reserved	s q	Reserved
40Ch	R p s s L	Reserved		
480h	Quadlet offset of the advanced feature CSR			
484h	Quadlet offset of the PIO control function CSR			
488h	Quadlet offset of the SIO control function CSR			
48Ch	Quadlet offset of the strobe output function CSR			
490h	Quadlet offset of the look up table function CSR			

Initial values	System dependent
Read values	System dependent (Depending on video format and video mode)
Write effect	Ignored

4.5 Inquiry register for feature elements

The following registers show the presence of features, modes and maximum value and minimum value for each feature. The camera, which supports multiple video, formats and video modes might change this registers. It is strongly recommended to check these registers every time the video format and/or video mode are changed. Some features may affect other features. Please see details in additional documents (the specific camera manual etc.) to determine which feature's status should be re-checked as a result.

The presence bits in the following registers shall have the same values as presence bits for the same feature in other registers (4xxh, 8xxh), at all times.

All the fields named xxx_Inq are bit assignments for inquiry. (0:Not available 1:Available)

(Definition and specification of each feature is described in Appendix A.)

Offset	Name	Field	Bit	Description
500h	BRIGHTNESS_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Capability of control with absolute value
		-	[2]	Reserved
		One_Push_Inq	[3]	One push auto mode (Controlled automatically by camera only once)
		ReadOut_Inq	[4]	Capability of reading the value of this feature
		On/Off_Inq	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto mode (Controlled automatically by camera)
		Manual_Inq	[7]	Manual mode (Controlled by user)
		Min_Value	[8..19]	Minimum value for this feature control
		Max_Value	[20..31]	Maximum value for this feature control
504h	AUTO_EXPOSURE_INQ	Same definition to BRIGHTNESS_INQ		
508h	SHARPNESS_INQ	Same definition to BRIGHTNESS_INQ		
50Ch	WHITE_BAL_INQ	Same definition to BRIGHTNESS_INQ		
510h	HUE_INQ	Same definition to BRIGHTNESS_INQ		
514h	SATURATION_INQ	Same definition to BRIGHTNESS_INQ		
518h	GAMMA_INQ	Same definition to BRIGHTNESS_INQ		
51Ch	SHUTTER_INQ	Same definition to BRIGHTNESS_INQ		
520h	GAIN_INQ	Same definition to BRIGHTNESS_INQ		
524h	IRIS_INQ	Same definition to BRIGHTNESS_INQ		
528h	FOCUS_INQ	Same definition to BRIGHTNESS_INQ		
52Ch	TEMPERATURE_INQ	Same definition to BRIGHTNESS_INQ		
530h	TRIGGER_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Capability of control with absolute value
		-	[2..3]	Reserved
		ReadOut_Inq	[4]	Capability of reading the value of this feature
		On/Off_Inq	[5]	Capability of switching this feature ON and OFF
		Polarity_Inq	[6]	Capability of changing polarity of the trigger input
		Value_Read_Inq	[7]	Capability of reading raw trigger input
		Trigger_Source0_Inq	[8]	Presence of Trigger Source 0 ID=0

		Trigger_Source1_Inq	[9]	Presence of Trigger Source 1	ID=1
		Trigger_Source2_Inq	[10]	Presence of Trigger Source 2	ID=2
		Trigger_Source3_Inq	[11]	Presence of Trigger Source 3	ID=3
		-	[12..14]	Reserved	ID=4-6
		Software_Trigger_Inq	[15]	Presence of Software Trigger	ID=7
		Trigger_Mode0_Inq	[16]	Presence of Trigger Mode 0	
		Trigger_Mode1_Inq	[17]	Presence of Trigger Mode 1	
		Trigger_Mode2_Inq	[18]	Presence of Trigger Mode 2	
		Trigger_Mode3_Inq	[19]	Presence of Trigger Mode 3	
		Trigger_Mode4_Inq	[20]	Presence of Trigger Mode 4	
		Trigger_Mode5_Inq	[21]	Presence of Trigger Mode 5	
		-	[22..29]	Reserved	
		Trigger_Mode14_Inq	[30]	Presence of Trigger Mode 14 (Vendor unique trigger 0)	
		Trigger_Mode15_Inq	[31]	Presence of Trigger Mode 15 (Vendor unique trigger 1)	
534h	TRIGGER_DLY_INQ	Same definition to BRIGHTNESS_INQ			
538h	WHITE_SHD_INQ	Same definition to BRIGHTNESS_INQ			
53Ch	FRAME_RATE_INQ	Same definition to BRIGHTNESS_INQ			
540h : 57Ch	Reserved for other FEATURE_HI_INQ				
580h	ZOOM_INQ	Presence_Inq	[0]	Presence of this feature	
		Abs_Control_Inq	[1]	Capability of control with absolute value	
			[2]	Reserved	
		One_Push_Inq	[3]	One push auto mode (Controlled automatically by camera only once)	
		ReadOut_Inq	[4]	Capability of reading the value of this feature	
		On/Off_Inq	[5]	Capability of switching this feature ON and OFF	
		Auto_Inq	[6]	Auto mode (Controlled automatically by camera)	
		Manual_Inq	[7]	Manual mode (Controlled by user)	
		Min_Value	[8..19]	Minimum value for this feature control	
		Max_Value	[20..31]	Max value for this feature control	
584h	PAN_INQ	Same definition to ZOOM_INQ			
588h	TILT_INQ	Same definition to ZOOM_INQ			
58Ch	OPTICAL_FILTER_INQ	Same definition to ZOOM_INQ			
590h : 5BCh	Reserved for other FEATURE_LO_INQ				
5C0h	CAPTURE_SIZE_INQ	Same definition to ZOOM_INQ			
5C4h	CAPTURE_QUALITY_INQ	Same definition to ZOOM_INQ			
5C8h : 5FCh	Reserved for other FEATURE_LO_INQ				

For TRIGGER_INQ

offset	0-7								8-15								16-23								24-31							
530h	p	a	R				r		o	p	v		0	1	2	3	R						s		0	1	2	3	4	5	Reserved						u	u

For others

offset	0-7								8-15								16-23								24-31							
5xxh	p	a	R			o			r			o			a			m							Min_Value							
	Max_Value																															

Initial values	System dependent
Read values	System dependent (Depend on video format and video mode)
Write effect	Ignored

4.6 Status and control registers for camera

Offset	Name	Bit	Description
600h	Cur_V_Frm_Rate / Revision	[0..2]	Current frame rate or revision for Format_6 FrameRate_0 .. FrameRate_7 / revision_0.. revision_7
	-	[3..31]	Reserved
604h	Cur_V_Mode	[0..2]	Current video mode Mode_0 .. Mode_7
	-	[3..5]	Reserved
	Cur_V_Mode_Hi	[6..7]	Extended Current video mode select. These two bits are for the selection of extended Format_7 video modes (Mode_8 to Mode_31). The Cur_V_Mode[0..2] and Cur_V_Mode_Hi[3..4] fields should be combined using the following bit order: (6,7,0,1,2). Mode_0 .. Mode_31 for Format_7 only
	-	[8..31]	Reserved
608h	Cur_V_Format	[0..2]	Current video format Format_0 .. Format_7
	-	[3..31]	Reserved
60Ch	ISO_Channel_L	[0..3]	Isochronous channel number for video data transmission of legacy mode (Except for Format_6) Available channel number is 0 to 15.
	-	[4..5]	Reserved
	ISO_Speed_L	[6..7]	Isochronous transmit speed code of legacy mode. (Except for Format_6) 0 = 100M 1 = 200M 2 = 400M
	-	[8..15]	Reserved
	Operation_Mode	[16]	1394 Operation Mode Change control register sets of ISO_Channel and ISO_Speed registers 0 = Legacy (v1.30 compatible) 1 = 1394.b (v1.3x mode) Camera shall start in legacy mode for backward compatibility.
	-	[17]	Reserved
	ISO_Channel_B	[18..23]	Isochronous channel number for video data transmission of 1394.b mode (Except for Format_6)
	-	[24..28]	Reserved
	ISO_Speed_B	[29..31]	Isochronous transmit speed code of 1394.b mode. (Except for Format_6) 0 = 100M 1 = 200M 2 = 400M 3 = 800M 4 = 1.6G 5 = 3.2G
610h	Camera_Power	[0]	1 = power-up camera 0 = power-down camera.
	-	[1..31]	Reserved

614h	ISO_EN/ Continuous_Shot	[0]	Except for Format_6: 1 = start ISO transmission of video data 0 = stop ISO transmission of video data For Format_6: 1 = start continuous shot and save to storage device. 0 = stop continuous shot If storage device becomes full, self cleared.
	-	[1..31]	Reserved
618h	Memory_Save	[0]	1 = current status and modes are saved to Mem_Save_Ch (Self Cleared)
	-	[1..31]	Reserved
61Ch	One_Shot / Retransmit	[0]	Except for Format_6: Live Mode (Transfer_Data_Select = 0): 1 = only one frame of video data is transmitted (Self cleared after transmission) Buffer Mode (Transfer_Data_Select = 1): 1 = Retransmit last frame (Self cleared after transmission) For Format_6: 1 = capture one image and save to storage device.(Self cleared) Ignored if ISO_EN = 1
	Multi_Shot / Image_Buffer_Read	[1]	Except for Format_6: Live Mode (Transfer_Data_Select = 0): 1 = N frames of video data is transmitted (Self cleared after transmission) Buffer Mode (Transfer_Data_Select = 1): 1 = N frames of buffered data is transmitted (Self cleared after transmission) N is Count_Number. See below. For Format_6: 1 = Capture N images and save to storage device(Self cleared). N is image number. See below. Ignored if ISO_EN = 1 or One_Shot = 1
	-	[2..15]	Reserved
	Count_Number	[16..31]	Count number for Multi_shot function.
620h	Mem_Save_Ch	[0..3]	Write channel for Memory_Save command Shall be >= 0001 (0 is factory settings, which cannot be overwritten) (See BASIC_FUNC_INQ)
	-	[4..31]	Reserved
624h	Cur_Mem_Ch	[0..3]	When read from, returns Current Memory Channel number When written to, loads status, modes, and values from the specified memory channel
	-	[4..31]	Reserved
628h	Vmode_Error_Status	[0]	Error status of combination of Video format, mode, frame rate and ISO_Speed setting. 0: no error 1: error This flag will be updated every time at one of the above setting is changed by writing new value. (Except for Format_6 and Format_7)
	-	[1..31]	Reserved

62Ch	Software_Trigger	[0]	Software trigger Write: 0: Reset software trigger 1: Set software trigger (Self cleared, when Trigger Mode=0,2,4) Read: 0: Ready 1: Busy
	-	[1..31]	Reserved
630h	Data_Depth	[0..7]	Effective data depth of current image data If read value of Data_Depth is zero, shall ignore this field. Write: Ignored Read: Effective data depth
	Little_Endian	[8]	Little endian mode for 16bit pixel formats only Has no effect if not in a 16bit pixel format Write/Read 0: Big endian mode (default on initialization) 1: Little endian mode
	-	[9..31]	Reserved
634h	Image_Buffer_Ctr	[0]	Image Buffer On/Off Control 0: OFF 1: ON The image buffer is initialized automatically when this bit is turned on
	Transfer_Data_Select	[1]	Transfer data path 0: Live data 1: Buffered image data Ignored if ISO_EN = 1
		[2 .. 7]	Reserved
	Max_Num_Images	[8..19]	Maximum number of images that can be stored in the current video format. Must be greater than zero. This field is read only.
	Number_of_Images	[20..31]	The number of images currently in the image buffer. This field is read only.

Initial values	System dependent.
Read values	Last update
Write effect	As indicated in table above

4.6.1.1 Transfer

During ISO_EN = 1 or One_Shot = 1 or Multi_Shot =1, the register value which reflects the Isochronous packet format cannot change. Writing value should be ignored. (Data transfer control priority is ISO_EN > One_Shot > Multi_Shot)

4.6.1.2 Image Buffer

Transmitting buffered data is available when ISO_EN = 0. Either One_shot or Multi_shot can be used to transmit buffered data when Transfer_Data_Select = 1. Multi_shot is used for transmitting one or more (as specified by Count_Number) buffered images. One_shot is used for retransmission of the last image from the retransmit buffer.

Image data shall be stored in a circular image buffer when Image_Buffer_Ctr = 1. If the circular buffer overflows, the oldest image in the buffer shall be overwritten.

Transmitted data shall always stored in the retransmit buffer. If a last or previous image does not exist, (for example an image has not been acquired since a video format or mode change), the camera shall still transmit an image from the retransmit buffer but its contents are undefined.

The image buffer shall be initialized when the Image_Buffer_Ctr is written to '1'. Changing the video format, video mode, image_size, or color_coding shall cause the image buffer to be initialized and Max_Num_Images field to be updated.

4.6.1.3 Data_Depth

This set of registers describes the effective data depth of the current image data. Unsigned image data should be filled from the least significant bit (LSB) and any remaining bits shall be filled with zeros. If the image data is signed, any remaining bits shall be sign extended. If the value of this register is zero, the camera doesn't support this feature and you shall ignore this value.

4.6.2 Storage Media CSR (only for Format_6)

Offset	Name	Field	Bit	Description
680h	Media_Status	Media_Presence	[0]	Presence of the Media. 1=presence (Read only)
		Write_Protect	[1]	1 = Write Protected, 0 = Writable
		-	[2..7]	Reserved
		Occupied_Rate	[8..15]	Percentage of occupied rate.(0x64=100d is full) (Read only)
		-	[16..31]	Reserved
684h	Number_Of_Images	Expected_Remain	[0..15]	Expected number of images can store If value is 0xffff, shall ignore this field. (Read only)
		Number_Of_Images	[16..31]	Number of stored images. (Read only)
688h	Media_Initialize	Initialize_Keyword	[0 ..31]	If the value that is equal to 'Initialize_Keyword' is written, media will be initialized. Initialize_Keyword = 0x46726D74 = 'Frmt'
68Ch	Image_ID for_Delete	Image_ID	[0..15]	Image_ID value to delete one image.
		-	[16..31]	Reserved
690h	Delete_Image	Delete_Keyword	[0..31]	If the value that is equal to 'Delete_Keyword' is written, one image it's ID is equal to "Image_ID" in 68Ch register will be deleted. Initialize_Keyword = 0x 44656C74 = 'Delt'

4.6.3 Stored Image CSR (only for Format_6)

Offset	Name	Field	Bit	Description
6C0h	Image_Number	Image_Number	[0..15]	Select one of the stored images. "Image_Number" shall be less than "Number_Of_Images" in 684h register.
		-	[16..31]	Reserved
6C4h	Image_Status	Write_Protect	[0]	1 = Write Protected, 0 = Writable
		-	[1..7]	Reserved
		Number_Of_Quality	[8..15]	This value shows number of image quality level in the selected image file. It shall be more than Zero. See "Load_Image_Quality" register. (Read Only)
		Image_ID	[15..31]	ID number of selected image. This is unique value in the same storage media. (Read only)
6C8h	Image_Information_Address	-	[0 ..15]	Reserved
		Address_Hi	[16..31]	Direct base address of the Image Information data. Upper 16 bits. (Read only)
6CCh	Image_Information_Address	Address_Lo	[0..31]	Direct base address of the Image Information data. Lower 32 bits. (Read only)
6D0h	Bytes_Of_Image_Information	Total_Bytes	[0..31]	Total amount of bytes of Image information data. If this value is Zero, information data for selected image is not available.
6D4h	Thumbnail_Address	-	[0 ..15]	Reserved
		Address_Hi	[16..31]	Direct base address of the thumbnail image data. Upper 16 bits. (Read only)
6D8h	Thumbnail_Address	Address_Lo	[0..31]	Direct base address of the thumbnail image data. Lower 32 bits. (Read only)
6DCh	Bytes_Of_Thumbnail	Total_Bytes	[0..31]	Total amount of bytes of thumbnail image data. If this value is Zero, thumbnail image of the selected image is not available. (Read only)
6E0h	Load_Image_Quality	Image_Quality	[0..7]	Select image quality level. 0 = whole data of the selected image file. 1 = lowest quality image data 'Image_Quality' <= 'Number_Of_Quality' Bigger value means higher quality.
6E4h	Image_Address	-	[0 ..15]	Reserved
		Address_Hi	[16..31]	Direct base address of the image data. Upper 16 bits. (Read only)
6E8h	Image_Address	Address_Lo	[0..31]	Direct base address of the image data. Lower 32 bits. (Read only)

6ECh	Bytes_Of_Image	Total_Bytes	[0..31]	Total amount of bytes of the image data. If this value is Zero, image is not available.

4.7 Status and control register for feature

The user can control each feature through "Status and control register for feature". The controllable items are mode and value.

The presence bits in the following registers shall have the same values as presence bits for the same feature in other registers (4xxh, 5xxh), at all times.

Mode:

Each CSR has three bits for mode control, ON_OFF, One_Push and A_M_Mode. A feature can have four states corresponding to the combination of mode control bits.

One_Push	ON_OFF	A_M_Mode	State
X	0	X	**Off state**. Feature will be fixed value state and uncontrollable.
X	1	1	**Auto control state**. Camera controls feature by itself continuously.
0	1	0	**Manual control state**. User can control feature by writing value to the value field.
1 (Self clear)	1	0	**One-Push action**. Camera controls feature by itself only once and return to Manual control state with adjusted value.

(X : don't care)

Value:

If ReadOut_Inq bit of the "Inquiry register for feature elements" is one, the value field is valid and can be used for controlling feature. The user can write control value to value field only at the Manual control state. At the other states, the user can only read the value. The camera always has to show the real setting value at the value field if ReadOut_Inq is one.

A camera, which supports multiple video, formats and video modes might change presence, capability mode, Min_Value and Max_Value of the feature. It is strongly recommended to check "Inquiry register for feature elements" register every time when you change the video format and/or video mode.

Offset	Name	Field	Bit	Description
800h	BRIGHTNESS	Presence_Inq	[0]	Presence of this feature 0:N/A 1:Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..4]	Reserved
		One_Push	[5]	Write '1': begin to work (Self cleared after operation) Read: Value='1' in operation Value='0' not in operation

				If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
		-	[8..19]	Reserved.
		Value	[20..31]	Value. Write the value in Auto or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
804h	AUTO_EXPOSURE	Same definition to BRIGHTNESS		
808h	SHARPNESS	Same definition to BRIGHTNESS		
80Ch	WHITE_BALANCE	Presence_Inq	[0]	Presence of this feature. 0:N/A 1:Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..4]	Reserved.
		One_Push	[5]	Write '1': begin to work (Self cleared after operation) Read: Value='1' in operation Value='0' not in operation If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
		U_Value / B_Value	[8..19]	U Value / B_Value. Write the value in AUTO or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no mean
		V_Value / R_Value	[20..31]	V Value / R_Value Write the value in AUTO or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no mean
810h	HUE	Same definition to BRIGHTNESS		
814h	SATURATION	Same definition to BRIGHTNESS		
818h	GAMMA	Same definition to BRIGHTNESS		
81Ch	SHUTTER	Same definition to BRIGHTNESS		
820h	GAIN	Same definition to BRIGHTNESS		
824h	IRIS	Same definition to BRIGHTNESS		
828h	FOCUS	Same definition to BRIGHTNESS		
82Ch	TEMPERATURE	Presence_Inq	[0]	Presence of this feature. 0:N/A 1:Available

		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..4]	Reserved.
		One_Push	[5]	Write '1': begin to work (Self cleared after operation) Read: Value='1' in operation Value='0' not in operation If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
		Target_ Temperature	[8..19]	Aimed value of the temperature. 10 times of the absolute temperature
		Temperature	[20..31]	Temperature at the present time. (Read only) 10 times of the absolute temperature
830h	TRIGGER_MODE	Presence_Inq	[0]	Presence of this feature. 0:N/A 1:Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..5]	Reserved.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		Trigger_Polarity	[7]	Select trigger polarity (Except for software trigger) If Polarity_Inq is "1", Write to change polarity of the trigger input Read to get polarity of the trigger input. If Polarity_Inq is "0", Read only. (0: Low active input, 1: High active input)
		Trigger_Source	[8..10]	Select trigger source Set trigger source ID from trigger source ID_Inq
		Trigger_Value	[11]	Trigger Input raw signal value Read only 0:Low, 1:High
		Trigger_Mode	[12..15]	Trigger mode. (Trigger_Mode_0..15)
		-	[16..19]	Reserved
		Parameter	[20..31]	Parameter for trigger function, if required. (Optional)

834h	TRIGGER_DELAY	Presence_Inq	[0]	Presence of this feature 0:N/A 1:Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..5]	Reserved
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		-	[7..19]	Reserved.
		Value	[20..31]	Value. Write the value in OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
838h	WHITE_SHADING	Presence_Inq	[0]	Presence of this feature 0:N/A 1:Available
		Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the Absolute value CSR If this bit = 1, value in the Value field is ignored.
		-	[2..4]	Reserved
		One_Push	[5]	Write '1': begin to work (Self cleared after operation) Read: Value='1' in operation Value='0' not in operation If A_M_Mode =1, this bit is ignored.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON If this bit =0, other fields will be read only.
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
		R-Value	[8-15]	Red channel compensation value. Write the value in Auto or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
		G-Value	[16-23]	Green channel compensation value. Write the value in Auto or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
		B-Value	[24-31]	Blue channel compensation value. Write the value in Auto or OFF mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
83Ch	FRAME_RATE	Same definition to BRIGHTNESS		

840h : 87Ch	Reserved for other FEATURE_HI	
880h	Zoom	Same definition to BRIGHTNESS
884h	PAN	Same definition to BRIGHTNESS
888h	TILT	Same definition to BRIGHTNESS
88Ch	OPTICAL_FILTER	Same definition to BRIGHTNESS
890h : 8BCh	Reserved for other FEATURE_LO	
8C0h	CAPTURE_SIZE	Same definition to BRIGHTNESS
8C4h	CAPTURE_QUALITY	Same definition to BRIGHTNESS
8C8h : 8FCh	Reserved for other FEATURE_LO	

For WHITE_BALANCE

offset	0-7						8-15	16-23	24-31
80Ch	p	a	R	o	o	a	U_Value / B_Value		V_Value / R_Value

For TEMPERATURE

offset	0-7						8-15	16-23	24-31
82Ch	p	a	R	o	o	a	Target_Temperature		Temperature

For TRIGGER_MODE

Offset	0-7					8-15			16-23	24-31
830h	p	a	R	o	p	T_S	v	T_Mode	R	Parameter

For TRIGGER_DELAY

Offset	0-7					8-15	16-23	24-31
834h	p	a	R	o	R	Reserved		Parameter

For WHITE_SHADING

Offset	0-7						8-15	16-23	24-31
838h	p	a	R	o	o	a	R-Value	G-Value	B-Value

For others

Offset	0-7						8-15	16-23	24-31
8xxh	p	a	R	o	o	a	Reserved		Value

Initial values	System dependent
Read values	Last update values
Write effect	Stored (bit [0] is read only)

4.7.1 Inquiry register for Absolute value CSR offset address

Offset	Name	Bit	Description
700h	ABS_CSR_HI_INQ_0	[0..31]	Quadlet offset of the Absolute value CSR for Brightness
704h	ABS_CSR_HI_INQ_1	[0..31]	Quadlet offset of the Absolute value CSR for Auto Exposure
708h	ABS_CSR_HI_INQ_2	[0..31]	Quadlet offset of the Absolute value CSR for Sharpness
70Ch	ABS_CSR_HI_INQ_3	[0..31]	Quadlet offset of the Absolute value CSR for White Balance
710h	ABS_CSR_HI_INQ_4	[0..31]	Quadlet offset of the Absolute value CSR for Hue
714h	ABS_CSR_HI_INQ_5	[0..31]	Quadlet offset of the Absolute value CSR for Saturation
718h	ABS_CSR_HI_INQ_6	[0..31]	Quadlet offset of the Absolute value CSR for Gamma
71Ch	ABS_CSR_HI_INQ_7	[0..31]	Quadlet offset of the Absolute value CSR for Shutter
720h	ABS_CSR_HI_INQ_8	[0..31]	Quadlet offset of the Absolute value CSR for Gain
724h	ABS_CSR_HI_INQ_9	[0..31]	Quadlet offset of the Absolute value CSR for Iris
728h	ABS_CSR_HI_INQ_10	[0..31]	Quadlet offset of the Absolute value CSR for Focus
72Ch	ABS_CSR_HI_INQ_11	[0..31]	Quadlet offset of the Absolute value CSR for Temperature
730h	ABS_CSR_HI_INQ_12	[0..31]	Quadlet offset of the Absolute value CSR for Trigger
734h	ABS_CSR_HI_INQ_13	[0..31]	Quadlet offset of the Absolute value CSR for Trigger Delay
738h	ABS_CSR_HI_INQ_14	[0..31]	Quadlet offset of the Absolute value CSR for White Shading
73Ch	ABS_CSR_HI_INQ_15	[0..31]	Quadlet offset of the Absolute value CSR for Frame Rate
740h : 77Fh	Reserved		
780h	ABS_CSR_LO_INQ_0	[0..31]	Quadlet offset of the Absolute value CSR for Zoom
784h	ABS_CSR_LO_INQ_1	[0..31]	Quadlet offset of the Absolute value CSR for Pan
788h	ABS_CSR_LO_INQ_2	[0..31]	Quadlet offset of the Absolute value CSR for Tilt
78Ch	ABS_CSR_LO_INQ_3	[0..31]	Quadlet offset of the Absolute value CSR for Optical Filter
790h : 7BFh	Reserved		
7C0h	ABS_CSR_LO_INQ_16	[0..31]	Quadlet offset of the Absolute value CSR for Capture Size
7C4h	ABS_CSR_LO_INQ_17	[0..31]	Quadlet offset of the Absolute value CSR for Capture Quality
7C8h : 7FFh	Reserved		

0-7	8-15	16-23	24-31
Base address of the Absolute value CSR (quadlet offset)			

"Base address of the Absolute value CSR" is the quadlet offset from the base address of initial register space.

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.7.2 Feature control error status register

Each field is an error or warning flag for the corresponding feature control register. If bit = 1, mode and/or value of the feature control register has some error or warning. If bit = 0, no error or warning. Each flag will be updated every time when corresponding feature control register is updated. It is strongly recommended to check feature register if bit = 1.

Offset	Name	Field	Bit	Description
640h	Feature_Control_Error_Status_HI	Brightness	[0]	Brightness Control
		Auto Exposure	[1]	Auto Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Speed Control
		Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13]	Trigger Delay Control
		White_Shading	[14]	White Shading Compensation Control
		Frame_Rate	[15]	Frame Rate Control
		-	[16..31]	Reserved
644h	Feature_Control_Error_Status_LO	Zoom	[0]	Zoom Control
		Pan	[1]	PAN Control
		Tilt	[2]	TILT Control
		Optical Filter	[3]	Optical Filter Control
		-	[4..15]	Reserved
		Capture_Size	[16]	Capture image size for Format_6
		Capture_Quality	[17]	Capture image quality for Format_6
		-	[18..31]	Reserved

Offset	0-7								8-15								16-23								24-31			
640h	b	e	s	w	h	s	g	s	g	l	f	t	t	t	w	f	Reserved											
644h	z	p	t	o	Reserved												s	g	Reserved									

Initial values	All zero
Read values	Last update
Write effect	Ignored

4.8 Register map

Offset	Register
000h	<Camera initialize register> INITIALIZE
100h 180h	<Inquiry register for video format> V_FORMAT_INQ <Inquiry register for video mode> V_MODE_INQ_x
200h	<Inquiry register for video frame rate> V_RATE_INQ_y_x
300h 360h	V_RATE_INQ_y_x continued <Reserved>
400h 480h	<Inquiry register for feature presence> BASIC_FUNC_INQ FEATURE_HI_INQ FEATURE_LO_INQ OPT_FUNCTION_INQ <Optional Function CSR offset>
500h	<Inquiry register for feature elements> xxxxxxxxxx_INQ
600h 640h 680h 6C0h	<Status and control register for camera> CAM_STA_CTRL <Feature control error status register> <Storage Media CSR> (Only for Format_6) <Stored Image CSR> (Only for Format_6)
700h	<Inquiry register for Absolute value CSR offset address>
800h	<Status and control register for feature> xxxxxxxxxxxx

4.9 Video Mode CSR for Format_7

Base address for each video mode command and status registers is:

Bus_ID, Node_ID , FFFF Fxxx xxxx (initial units space)

This address is contained in the Format_7 section of the "4.2.3 Inquiry register for video frame rate and base address of the Video Mode CSR for the Partial Image Size Format". This register shall be prepared for each video mode that is Format_7, Mode_x.

The offset field in each of the following table is the byte offset from the above base address.

Offset	Name	Field	Bit	Description	
000h	MAX_IMAGE_SIZE_INQ	Hmax	[0..15]	Maximum Horizontal pixel number	
		Vmax	[16..31]	Maximum Vertical pixel number	
004h	UNIT_SIZE_INQ	Hunit	[0..15]	Horizontal unit pixel number	
		Vunit	[16..31]	Vertical unit pixel number	
008h	IMAGE_POSITION	Left	[0..15]	Left position of requested image region (pixels)	
		Top	[16..31]	Top position of requested image region (pixels)	
00Ch	IMAGE_SIZE	Width	[0..15]	Width of requested image region (pixels)	
		Height	[16..31]	Height of requested image region (pixels)	
010h	COLOR_CODING_ID	Coding_ID	[0..7]	Color coding ID from COLOR_CODING_INQ register	
		-	[8..31]	Reserved	
014h	COLOR_CODING_INQ	Mono8	[0]	Y only. Y=8bits, non compressed	ID=0
		4:1:1 YUV8	[1]	4:1:1, Y=U=V= 8bits, non compressed	ID=1
		4:2:2 YUV8	[2]	4:2:2, Y=U=V=8bits, non compressed	ID=2
		4:4:4 YUV8	[3]	4:4:4, Y=U=V=8bits, non compressed	ID=3
		RGB8	[4]	R=G=B=8bits, non compressed	ID=4
		Mono16	[5]	Y only, Y=16bits, non compressed (unsigned integer)	ID=5
		RGB16	[6]	R=G=B=16bits, non compressed (unsigned integer)	ID=6
		Signed Mono16	[7]	Y only, Y=16bits, non compressed (signed integer)	ID=7
		Signed RGB16	[8]	R=G=B=16bits, non compressed (signed integer)	ID=8
		Raw8	[9]	Raw data output of color filter sensor, 8bits	ID=9
		Raw16	[10]	Raw data output of color filter sensor, 16bits	ID=10
		Mono12	[11]	Y only, Y=12bits, non compressed (unsigned integer)	ID=11
		Raw12	[12]	Raw data output of color filter sensor, 12 bits	ID=12
		-	[13..31]	Reserved	ID= 13-31
018h : 023h	COLOR_CODING_INQ	Reserved for other Color_Coding.			ID= 32-127

024h : 033h	COLOR_CODING_INQ	Vendor Unique Color_Coding 0-127			ID= 128-255
034h	PIXEL_NUMBER_INQ	PixelPerFrame	[0..31]	Pixel number per frame	
038h	TOTAL_BYTES_HI_INQ	BytePerFrameHi	[0..31]	Higher quadlet of total bytes of image data per frame	
03Ch	TOTAL_BYTES_LO_INQ	BytePerFrameLo	[0..31]	Lower quadlet of total bytes of image data per frame	
040h	PACKET_PARA_INQ	UnitBytePerPacket	[0..15]	Unit (Minimum) bytes per packet Multiple by 4	
		MaxBytePerPacket	[16..31]	Maximum bytes per packet Multiple by UnitBytePerPacket	
044h	BYTE_PER_PACKET	BytePerPacket	[0..15]	Packet size	
		RecBytePerpacket	[16..31]	Recommended bytes per packet. If this value is zero, shall ignore this field.	
048h	PACKET_PER_FRAME_INQ	PacketPerFrame	[0..31]	Number of Packets per frame. If this value is zero, the host shall calculate PacketPerFrame itself.	
04Ch	UNIT_POSITION_INQ	Hposunit	[0..15]	Horizontal unit pixel number for position If read value of Hposunit is 0, Hposunit = Hunit for compatibility.	
		Vposunit	[16..31]	Vertical unit number for position If read value of Vposunit is 0, Vposunit = Vunit for compatibility.	
050h	FRAME_INTERVAL_INQ	FrameInterval	[0..31]	Current Frame interval (sec) (IEEE/REAL*4 Floating-Point Value) If read value of Frame_Interval is zero, shall ignore this field.	
054h	DATA_DEPTH_INQ	DataDepth	[0..7]	Effective image data depth of this mode If read value of Data_Depth is zero, shall ignore this field.	
		-	[8..31]	Reserved	
058h	COLOR_FILTER_ID		[0..7]	RGB primary color filter (RG/GB)	ID = 0
				RGB primary color filter (GB/RG)	ID = 1
				RGB primary color filter (GR/BG)	ID = 2
				RGB primary color filter (BG/GR)	ID = 3
				Reserved for other color filter	ID = 4 : ID=127
				Vendor unique color filter 0	ID=128
				Vendor unique color filter 1	ID=129
				:	:
				Vendor unique color filter 126	ID=254
				Vendor unique color filter 127	ID=255
		-	[8..31]	Reserved	
05Ch : 07Bh	Reserved				
07Ch	VALUE_SETTING	Presence	[0]	If this bit is one, "Setting_1", "ErrorFlag_1" and "ErrorFlag_2" fields are valid. This bit is read only.	

		Setting_1	[1]	If writing "1" to this bit, IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register value will be reflected in PIXEL_NUMBER_INQ, TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET register. This bit is self-cleared. The user should wait for it to become 0 then checking ErrorFlag_1 is zero before using the value in the PIXEL_NUMBER_INQ, TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET register
		-	[2..7]	Reserved
		ErrorFlag_1	[8]	Combination of the values of IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register is not acceptable. 1: error 0: no error This flag will be updated every time when Setting_1 bit returns to "0" from "1".
		ErrorFlag_2	[9]	BytePerPacket value is not acceptable. 1: error 0: no error
		-	[10..31]	Reserved

During ISO_EN = 1 or One_Shot = 1 or Multi_Shot =1, the register value which reflects the Isochronous packet format cannot change. Writing value should be ignored.

4.9.1 MAX_IMAGE_SIZE_INQ register

This register is an inquiry register for maximum image size.

0-7	8-15	16-23	24-31
Hmax (pixels)		Vmax (pixels)	

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.9.2 UNIT_SIZE_INQ and UNIT_POSITION_INQ register

This register is an inquiry register for unit size.

Hmax = Hunit * n = Hposunit*n3 (n, n3 is integer)

Vmax = Vunit * m = Vposunit*m3 (m, m3 is integer)

If read value of Hposunit is 0, Hposunit = Hunit for compatibility with Rev 1.20.

If read value of Vposunit is 0, Vposunit = Vunit for compatibility with Rev 1.20.

UNIT_SIZE_INQ

0-7	8-15	16-23	24-31
Hunit (pixels)		Vunit (pixels)	

UNIT_POSITION_INQ

0-7	8-15	16-23	24-31
Hposunit (pixels)		Vposunit (pixels)	

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.9.3 IMAGE_POSITION and IMAGE_SIZE register

These registers determine an area of required data. All the data shall be as follows:

Left = Hposunit * n1

Top = Vposunit * m1

Width = Hunit * n2

Height = Vunit * m2 (n1, n2, m1, m2 are integer)

Left + Width <= Hmax

Top + Height <= Vmax

0-7	8-15	16-23	24-31
Left		Top	

0-7	8-15	16-23	24-31
Width		Height	

Initial values	System dependent
Read values	Last update value
Write effect	Stored

4.9.4 COLOR_CODING_ID and COLOR_CODING_INQ registers

COLOR_CODING_INQ register describes available color-coding capability of the system. Each coding scheme has its own ID number. Required color-coding scheme shall be set to COLOR_CODING_ID register as the ID number.

COLOR_CODING_ID register

0-7	8-15	16-23	24-31
Coding_ID	Reserved		

Initial values	System dependent
Read values	Last update value
Write effect	Stored

COLOR_CODING_INQ registers

0-7	8-15	16-23	24-31
Bit assignment is described in the table above			

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

4.9.5 PIXEL_NUMBER_INQ and TOTAL_BYTE_INQ registers

PIXEL_NUMBER_INQ register includes total pixel number of required image area.

TOTAL_BYTE_INQ register includes total data amount value of required image area as the bytes. If Presence bit in the VALUE_SETTING register is zero, values of these registers will be updated by writing new value to IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers. If Presence bit in the VALUE_SETTING register is one, values of these registers will be updated by writing one to the Setting_1 bit in the VALUE_SETTING register. If ErrorFlag_1 bit is zero after Setting_1 bit returns to zero, values of these registers are valid.

PacketPerFrame * BytePerPacket indicates whole data size include padding data.

Caution: TotalByte indicates effective image data size. It doesn't include padding data.

PIXEL_NUMBER_INQ register

0-7	8-15	16-23	24-31
PixelPerFrame			

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

TOTAL_BYTE_HI_INQ and TOTAL_BYTE_LO_INQ registers

0-7	8-15	16-23	24-31
Higher part of BytePerFrame			
Lower part of BytePerFrame			

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

4.9.6 PACKET_PARA_INQ and BYTE_PER_PACKET register

MaxBytePerPacket describes maximum packet size for one Isochronous packet.
UnitBytePerPacket is the unit for Isochronous packet size.

RecBytePerPacket describes recommended packet size for one Isochronous packet. If RecBytePerPacket is zero, you shall ignore this field.

If Presence bit in the VALUE_SETTING register is zero, values of these fields will be updated by writing new value to IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers with the value of ISO_Speed register.

At first, ISO_Speed register shall be written. Then IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers should be updated.

If Presence bit in the VALUE_SETTING register is one, values of these fields will be updated by writing one to the Setting_1 bit in the VALUE_SETTING register. If ErrorFlag_1 bit is zero after Setting_1 bit returns to zero, values of these fields are valid.

BytePerPacket value determines real packet size and transmission speed for one frame image. BytePerPacket value shall keep the following condition.

BytePerPacket = UnitBytePerPacket * n (n is integer) BytePerPacket <= MaxBytePerPacket

PACKET_PARA_INQ

0-7	8-15	16-23	24-31
UnitBytePerPacket		MaxBytePerPacket	

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

BYTE_PER_PACKET

0-7	8-15	16-23	24-31
BytePerPacket		RecBytePerPacket	

For RecBytePerPacket field

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

For BytePerPacket field

Initial values	System dependent
Read values	Last update value
Write effect	Stored

4.9.7 PACKET_PER_FRAME_INQ register

If BytePerPacket * n != BytePerFrame (n is integer), you shall use padding. The PacketPerFrame value is a number of packets per one frame. This register will be updated after BytePerPacket is written. If the value is zero, the host shall calculate PacketPerFrame itself. PacketPerFrame can be calculated by " TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ" and " BYTE_PER_PACKET ". Total number of bytes of transmission data per one frame = BytePerPacket * PacketPerFrame

Number of bytes of padding = BytePerPacket * PacketPerFrame - BytePerFrame

Receiver shall ignore above padding data in the last packet of each frame.

The host program shall calculate PacketPerFrame as follows.

```
if( TotalByte % BytePerPacket == 0) {
  PacketPerFrame = TotalByte / BytePerPacket;
} else {
  PacketPerFrame = TotalByte / BytePerPacket + 1;
```

}

0-7	8-15	16-23	24-31
PacketPerFrame			

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

4.9.8 VALUE_SETTING register

If Presence bit is one, this register is available and valid. Purpose of Setting_1 bit is for updating TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET register. If one of the value in the IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register is changed, Setting_1 bit shall be set "1".

ErrorFlag_1 field will be updated when Setting_1 bit returns to "0". If ErrorFlag_1 field is zero, values of TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET register are valid.

After the BytePerPacket value is written, the ErrorFlag_2 field will be updated. If ErrorFlag_2 is zero, Isochronous transmission can be started without any problem.

0-7			8-31		
p	s	Reserved	e	e	Reserved

For Presence

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

For Setting_1

Initial values	System dependent
Read values	Last update value
Write effect	Stored and self clear

For ErrorFlag_1, ErrorFlag_2

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

4.9.9 FRAME_INTERVAL_INQ register

This describes status of frame interval of current camera conditions including exposure time. Reciprocal value of this is frame rate of the camera. If value of this register is zero, camera can't report this value you shall ignore this value. Frame_Interval is defined by sec in IEEE1394/REAL*4 floating-point value.

0-7	8-15	16-23	24-31
Frame_Interval			

Initial values	System dependent
Read values	Last update value
Write effect	Ignored

4.9.10 DATA_DEPTH_INQ register

This indicates effective image data depth of this mode. Image data should be filled from least significant bit (LSB) and odd bits should be filled with zeros. If the value of this register is zero, the camera doesn't support this feature and you shall ignore this value.

0-7	8-15	16-23	24-31
Data_Depth	Reserved		

Initial values	System dependent
Read values	System dependent
Write effect	Ignored

4.9.11 COLOR_FILTER_ID register

This describes color filter arrangement ID of color-filtered sensors.

0-7	8-15	16-23	24-31
Color_Filtrer_ID	Reserved		

Initial values	System dependent
Read values	Same as initial value
Write effect	Ignored

4.10 CSRs Advanced Features

These CSRs are for vendor unique features. The vendor shall prepare CSRs for these additional features and write the base address of these CSRs at 480h as a quadlet offset value from the base address of initial register space.

The first two quadlets are "Access Control Register"(ACR). The user has to write "Feature_ID" to ACR to unlock "CSRs Advanced Features". Each model that implements "CSRs Advanced Features" shall have "Feature_ID". "Feature_ID" is advanced feature set unique value and consists of 48bits.

The remaining structure of this area has to be determined by vendor.

The user can determine Time_Out value with the unlock operation. Time_Out value consists of 12 bits and the unit is millisecond. (Maximum 4.095 second) If the user does not access "CSRs Advanced Features" within Time_Out value, the unlock operation will be canceled and ACR will return to its initial state. If the user access "CSRs Advanced Features" within Time_Out value, Time_out will be refreshed. If this value is “0”, Time_Out doesn’t occur. (Can access any vendor unique register anytime.)

1) After unlocked, if response of reading Bus_ID+Node_ID field is user node's ID, and only unlocking node can access "CSRs Advanced Features" within time-out. (Node locked mode)

2) After unlocked, if response of reading Bus_ID+Node_ID field is camera's own ID, and not only unlocking node but also other nodes also can access "CSRs Advanced Features" within time-out. (Unlocked mode)

If bus reset occurs, ACR will be initialized.

Access Control Register

Write format

<table>
<tr><td>0-7</td><td>8-15</td><td>16-23</td><td>24-31</td></tr>
<tr><td colspan="4">Feature_ID_Hi</td></tr>
<tr><td colspan="2">Feature_ID_Lo</td><td>0xf</td><td>Time_Out</td></tr>
</table>

Read format

<table>
<tr><td>0-7</td><td>8-15</td><td>16-23</td><td>24-31</td></tr>
<tr><td colspan="2">Bus_ID+Node_ID</td><td colspan="2">0xffff</td></tr>
<tr><td colspan="3">0xffffff</td><td>Time_Out</td></tr>
</table>

Initial values	All ones (0xffffffffffffffff)
Read values	Last update value
Write effect	If the upper 48 bits of written value is equal to "Feature_ID", store source or target (depend on lock mode) Bus_ID + Node_ID (16 bits) value to upper 16bits area. Also, Time_Out value and lower 12 bits value are stored. If Time_Out value= “0”, no time out occurs. The other bits will be one. If upper 48 bits of written value is not equal to "Feature_ID", write action is ignored and all bits will be one.
Bus Reset	All one

Feature_ID

0-7	8-15	16-23	24-31	32-39	40-47
Company_ID			Advanced feature set unique value		

Each company has to manage lower 3 bytes value to keep advanced feature set uniqueness.

4.11 Optional Function CSR

4.11.1 PIO Control Function

These CSRs are for parallel input/output (PIO) control function. PIO is a general input and output parallel port via camera.

Offset	Name	Field	Bit	Description
000h	PIO_Output	Output_Port	[0..31]	General purpose PIO output
004h	PIO_Input	Input_Port	[0..31]	General purpose PIO input

4.11.2 SIO Control Function

These CSRs are for serial input/output (SIO) control function. SIO is a general input and output serial port via camera.

4.11.2.1 Serial Input Transaction

[1] Read the valid data size of current receive buffer RBUF_ST_CNT or RDRD flag.

[2] Write the input data length to RBUF_ST_CNT.

[3] Read received characters from SIO_Data_Register.

[4] To input more characters, repeat from step 1.

Note) Overrun read data value of the receive buffer are undefined.

4.11.2.2 Serial Output Transaction

[1] Read the available data space of current transmit buffer TBUF_ST_CNT or TDRD flag.

[2] Write characters to SIO_Data_Register

[3] Write the valid output data length to TBUF_ST_CNT to start transmit

[4] To output more characters, repeat from step 1.

Note 1) Padding data in the transmit buffer is discarded after a successful output transaction. (If OUTPUT_LENGTH=1 and write a quadlet (4-byte) data to SERIAL_DATA_BUFFER, only first char is transmitted and remaining 3 chars are discarded from buffer).

Note 2) Transmitted data may be discarded from buffer.

Offset	Name	Field	Bit	Description
000h	Serial_Mode_Reg	Baud Rate	[0..7]	Baud Rate setting Write: Set baud rate Read: Get current baud rate 0: 300bps 1: 600bps 2: 1200bps 3: 2400bps 4: 4800bps 5: 9600bps 6: 19200bps 7: 38400bps 8: 57600bps 9: 115200bps 10: 230400bps Other values reserved
		Char_Length	[8..15]	Character length setting Write: Set data length (must not be 0) Read: Get data length 7: 7bits 8: 8bits Other values reserved
		Parity	[16..17]	Parity setting Write: Set parity Read: Get current parity 0: None 1: Odd 2: Even
		Stop_Bit	[18..19]	Stop bits Write: Set stop bit Read: Get current stop bit 0: 1 1: 1.5 2: 2
		-	[20..23]	Reserved
		Buffer_Size_Inq	[24..31]	Buffer Size (Read Only) This field indicates the maximum size of receive/transmit data buffer If this value=1, Buffer_Status_Control, SIO_Data_Register Char1-3 should be ignored.
004h	Serial_Contol _Reg	RE	[0]	Receive enable Read: Current status Write: 0:Diasable 1:Enable
		TE	[1]	Transmit enable Read: Current status Write: 0:Diasable 1:Enable
		-	[2..7]	Reserved

	Serial_Status_Reg	TDRD	[8]	Transmit data buffer ready Read only 0: Not ready 1:Ready
		-	[9]	Reserved
		RDRD	[10]	Receive data buffer ready Read only 0:Not ready 1:Ready
		-	[11]	Reserved
		ORER	[12]	Receive buffer over run error Read: Current status Write: 0:Clear flag 1:Ignored
		FER	[13]	Receive data framing error Read: Current status Write: 0:Clear flag 1:Ignored
		PER	[14]	Receive data parity error Read: Current status Write: 0:Clear Flag 1:Ignored
		-	[15]	Reserved
008h	Receive_Buffer_Status_Control	RBUF_ST	[0..8]	SIO receive buffer status Read: Valid data size of current receive buffer Write: Ignored
		RBUF_CNT	[8..15]	SIO receive buffer control Read: Remain data size for read Write: Set input data size
		-	[16::31]	Reserved
00Ch	Transmit_Buffer_Status_Control	TBUF_ST	[0..7]	SIO output buffer status Read: Available data space of transmit buffer Write: Ignored
		TBUF_CNT	[8..15]	SIO output buffer control Read: Written data size to buffer Write: Set output data size for transmit
		-	[16..31]	Reserved
010h : 0FFh				Reserved
100h	SIO_Data_Register	Char_0	[0..7]	Character_0 Read: Read character from receive buffer Padding data, if data is not available Write: Write character to transmit buffer Padding data, if data is invalid
		Char_1	[8..15]	Character_1 Read: Read character from receive buffer+1 Padding data, if data is not available Write: Write character to transmit buffer+1 Padding data, if data is invalid

		Char_2	[16..23]	Character_2 Read: Read character from receive buffer+2 Padding data, if data is not available Write: Write character to transmit buffer+2 Padding data, if data is invalid
		Char3	[17..31]	Character_3 Read: Read character from receive buffer+3 Padding data, if data is not available Write: Write character to transmit buffer+3 Padding data, if data is invalid
104h : 1FFH	SIO_Data_Register_Alias		[0..31]	Alias SIO_Data_Register area for block transfer

4.11.3 Strobe Signal Output Function

These CSRs are for the strobe signal output function. Strobe signal is a timing output signal with shutter start. Each strobe signal is defined by delay after shutter start and pulse duration.

Offset	Name	Field	Bit	Description
000h	Strobe_CTRL_Inq	Strobe_0_Inq	[0]	Presence of strobe 0 signal
		Strobe_1_Inq	[1]	Presence of strobe 1 signal
		Strobe_2_Inq	[2]	Presence of strobe 2 signal
		Strobe_3_Inq	[3]	Presence of strobe 3 signal
		-	[4..31]	Reserved
004h : 0FCh	Reserved			
100h	Strobe_0_Inq	Presence_Inq	[0]	Presence of this function
			[1..3]	Reserved
		ReadOut_Inq	[4]	Capability of reading the value of this feature
		On/Off_Inq	[5]	Capability of switching this function ON and OFF
		Polarity_Inq	[6]	Capability of changing polarity of the signal
			[7]	Reserved
		Min_Value	[8..19]	Minimum value of this function control
		Max_Value	[20..31]	Maximum value of this function control
104h	Strobe_1_Inq	Same definition to Strobe_0_Inq		
108h	Strobe_2_Inq	Same definition to Strobe_1_Inq		
10Ch	Strobe_3_Inq	Same definition to Strobe_2_Inq		
110h : 1FCh	Reserved			
200h	Strobe_0_Cnt	Presence_Inq	[0]	Presence of this function. 0:N/A 1:Available
		-	[1..5]	Reserved.
		ON_OFF	[6]	Write: ON or OFF this function, Read: read a status 0: OFF, 1: ON

				If this bit =0, other fields will be read only.
		Signal_Polarity	[7]	Select signal polarity If Polarity_Inq is "1", Write to change polarity of the strobe output Read to get polarity of the strobe output. If Polarity_Inq is "0", Read only. (0: Low active output, 1: High active output)
		Delay_Value	[8..19]	Delay after start of exposure until the strobe signal asserts.
		Duration_Value	[20..31]	Duration of the strobe signal. A value 0 means dessert at the end of exposure function, if required.
204h	Strobe_1_Cnt	Same definition to Strobe_1_Cnt		
208h	Strobe_2_Cnt	Same definition to Strobe_2_Cnt		
20Ch	Strobe_3_Cnt	Same definition to Strobe_3_Cnt		
210h : 2FFh	Reserved			

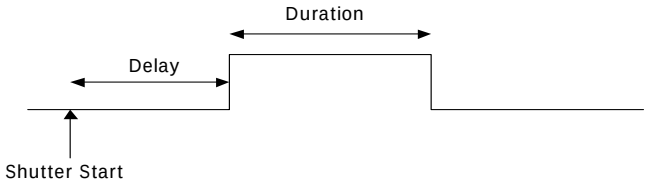


Figure 5 – Strobe Signal Output

4.11.4 Look Up Table Function

These CSRs are for the look up table function. The look up table function can define up to 16 banks where each bank can contain up to 16 channels. Each channel shall define a table with a length of 2^{Input_Depth} entries where each entry is Output_Depth bits wide. Channel table entries shall be padded to 32 bits or a complete quadlet.

Each bank may be read only, write only or both read and write capable as shown by the LUT_Bank_Rd_Inq and LUT_Bank_Wr_Inq fields. The active bank shall be set by writing to the ACTIVE_BANK field of the LUT_Ctrl register.

The Bank_X_Offset_Inq register shall give the offset to start address of the array of channel tables in each bank. Multiple channels can be used to process color video pixel data.

The effect of the look up table function on video pixel data is defined by the camera vendor.

Offset	Name	Field	Bit	Description
000h	LUT_Ctrl_Inq (Read Only)	Presence_Inq	[0]	Presence of this feature 0:N/A 1:Available
		-	[1..4]	Reserved
		ON_OFF_Inq	[5]	Capability of turning this feature ON or OFF.
		-	[6..7]	Reserved
		Input_Depth	[8..12]	Input data bit depth

		Output_Depth	[13..17]	Output data bit depth
		-	[18]	Reserved
		Number_of_Channels	[19..23]	Number of channels
		-	[24..26]	Reserved
		Number_of_Banks	[27..31]	Number of banks
004h	LUT_Bank_Rd_Inq	Read_Bank_0_Inq	[0]	Capability of reading data from Bank 0
		Read_Bank_1_Inq	[1]	Capability of reading data from Bank 1
		Read_Bank_2_Inq	[2]	Capability of reading data from Bank 2
		Read_Bank_3_Inq	[3]	Capability of reading data from Bank 3
		Read_Bank_4_Inq	[4]	Capability of reading data from Bank 4
		Read_Bank_5_Inq	[5]	Capability of reading data from Bank 5
		Read_Bank_6_Inq	[6]	Capability of reading data from Bank 6
		Read_Bank_7_Inq	[7]	Capability of reading data from Bank 7
		Read_Bank_8_Inq	[8]	Capability of reading data from Bank 8
		Read_Bank_9_Inq	[9]	Capability of reading data from Bank 9
		Read_Bank_10_Inq	[10]	Capability of reading data from Bank 10
		Read_Bank_11_Inq	[11]	Capability of reading data from Bank 11
		Read_Bank_12_Inq	[12]	Capability of reading data from Bank 12
		Read_Bank_13_Inq	[13]	Capability of reading data from Bank 13
		Read_Bank_14_Inq	[14]	Capability of reading data from Bank 14
		Read_Bank_15_Inq	[15]	Capability of reading data from Bank 15
	LUT_Bank_Wr_Inq	Write_Bank_0_Inq	[16]	Capability of writing data to Bank 0
		Write_Bank_1_Inq	[17]	Capability of writing data to Bank 1
		Write_Bank_2_Inq	[18]	Capability of writing data to Bank 2
		Write_Bank_3_Inq	[19]	Capability of writing data to Bank 3
		Write_Bank_4_Inq	[20]	Capability of writing data to Bank 4
		Write_Bank_5_Inq	[21]	Capability of writing data to Bank 5
		Write_Bank_6_Inq	[22]	Capability of writing data to Bank 6
		Write_Bank_7_Inq	[23]	Capability of writing data to Bank 7
		Write_Bank_8_Inq	[24]	Capability of writing data to Bank 8
		Write_Bank_9_Inq	[25]	Capability of writing data to Bank 9
		Write_Bank_10_Inq	[26]	Capability of writing data to Bank 10
		Write_Bank_11_Inq	[27]	Capability of writing data to Bank 11
		Write_Bank_12_Inq	[28]	Capability of writing data to Bank 12
		Write_Bank_13_Inq	[29]	Capability of writing data to Bank 13
		Write_Bank_14_Inq	[30]	Capability of writing data to Bank 14
		Write_Bank_15_Inq	[31]	Capability of writing data to Bank 15
008h	LUT_Ctrl	Presence_Inq	[0]	Presence of this Feature 0: N/A 1: Available
		-	[1..4]	Reserved
		ON_OFF	[5]	Write: ON or OFF this feature Read: read a status 0: OFF 1: ON
		-	[6..27]	Reserved
		Active_Bank	[28..31]	Active bank
00Ch	Bank_0_Offset_Inq	Bank_0_Quadlet_Offset	[0..31]	Quadlet offset of Bank 0 table data
010h	Bank_1_Offset_Inq	Bank_1_Quadlet_Offset	[0..31]	Quadlet offset of Bank 1 table data
014h	Bank_2_Offset_Inq	Bank_2_Quadlet_Offset	[0..31]	Quadlet offset of Bank 2 table data
018h	Bank_3_Offset_Inq	Bank_3_Quadlet_Offset	[0..31]	Quadlet offset of Bank 3 table data
01Ch	Bank_4_Offset_Inq	Bank_4_Quadlet_Offset	[0..31]	Quadlet offset of Bank 4 table data
020h	Bank_5_Offset_Inq	Bank_5_Quadlet_Offset	[0..31]	Quadlet offset of Bank 5 table data
024h	Bank_6_Offset_Inq	Bank_6_Quadlet_Offset	[0..31]	Quadlet offset of Bank 6 table data
028h	Bank_7_Offset_Inq	Bank_7_Quadlet_Offset	[0..31]	Quadlet offset of Bank 7 table data

02Ch	Bank_8_Offset_Inq	Bank_8_Quadlet_Offset	[0..31]	Quadlet offset of Bank 8 table data
030h	Bank_9_Offset_Inq	Bank_9_Quadlet_Offset	[0..31]	Quadlet offset of Bank 9 table data
034h	Bank_10_Offset_Inq	Bank_10_Quadlet_Offset	[0..31]	Quadlet offset of Bank 10 table data
038h	Bank_11_Offset_Inq	Bank_11_Quadlet_Offset	[0..31]	Quadlet offset of Bank 11 table data
03Ch	Bank_12_Offset_Inq	Bank_12_Quadlet_Offset	[0..31]	Quadlet offset of Bank 12 table data
040h	Bank_13_Offset_Inq	Bank_13_Quadlet_Offset	[0..31]	Quadlet offset of Bank 13 table data
044h	Bank_14_Offset_Inq	Bank_14_Quadlet_Offset	[0..31]	Quadlet offset of Bank 14 table data
048h	Bank_15_Offset_Inq	Bank_15_Quadlet_Offset	[0..31]	Quadlet offset of Bank 15 table data

4.11.4.1 Lookup Table Data Structure

Each bank of channels shall be composed of entries padded to a complete 32-bit quadlet. Each bank shall be organized as show in the table below.

Cn: Channel Number

En : Entry Number

C(0)E(0) … … C(0)E(2^{Input_Depth}-1)
C(1)E(0) … … C(1)E(2^{Input_Depth}-1)
… … …
C(Number_of_Channels-1)E(0) … … C(Number_of_Channels-1) E(2^{Input_Depth}-1)

4.12 Absolute value CSR for Feature elements

Absolute value CSR is for absolute value control for each feature elements if available. Each CSR consists of three quadlet. Vendor shall prepare CSR and write base address of this CSR at "Inquiry register for Absolute value CSR offset address" as a quadlet offset value from the base address of initial register space.

Units of all elements are predefined. Please see appendix B for details.

All value shall be IEEE/REAL*4 Floating-point format.

Offset	Name	Field	Bit	Description
000h	Absolute value	Min_Value	[0..31]	Minimum value for this feature control
004h		Max_Value	[0..31]	Maximum value for this feature control
008h		Value	[0..31]	Absolute control value

0-7	8-15	16-23	24-31
Floating-point value with IEEE/REAL*4 format			

IEEE/REAL*4 Floating-Point Value Notation:

Value = (-1)**S * 1.mmmmmmmmmmmmmmmmmmmmmmm * 2**(exp-127)

Sign (S)	Exponent (exp)	Mantissa (m)
1bit	8bit	23bit

For Min_Value, Max_Value

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

For Value

Initial values	System dependent
Read values	Real setting value
Write effect	Stored but adjusted to real setting value

5 Isochronous packet format

Every video format, mode and frame rate has different video data format.

5.1 Isochronous packet format for Format_0, Format_1 and Format_2

5.1.1 Video Isochronous packet structure

The following table shows the format of the first quadlet in the data field of each Isochronous data block.

0-7	8-15	16-23		24-31	
data_length		tg	channel	tCode	sy
header_CRC					
Video data payload					
data_CRC					

Isochronous Data Block Packet Format

Where the following fields are defined in the IEEE 1394 standard:

data_length : number of bytes in the data field

tg : (tag field) shall be set to zero

channel : isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register

tCode : (transaction code) shall be set to the isochronous data block packet tCode

sy : (synchronization value) shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous data blocks

Video data payload: shall contain the digital video information, as defined in the following sections

5.1.2 Video mode comparison chart

Format_0

Mode	Video Format	240fps	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
Mode_0	160x120 YUV(4:4:4) 24bit/pixel	4H 640p 480q	2H 320p 240q	1H 160p 120q	1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q		
Mode_1	320x240 YUV(4:2:2) 16bit/pixel	8)8H 2560p 1280q	4)4H 1280p 640q	2H 640p 320q	1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q	1/16H 20p 10q
Mode_2	640x480 YUV(4:1:1) 12bit/pixel	16)16H 10240p 3840q	8)8H 5120p 1920q	4)4H 2560p 960q	2) 2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q	1/8H 80p 30q
Mode_3	640x480 YUV(4:2:2) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4) 2H 1280p 640q	2) 1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
Mode_4	640x480 RGB 24bit/pixel	32)16H 10240p 7680q	16)8H 5120p 3840q	8)4H 2560p 1920q	4) 2H 1280p 960q	2) 1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q	1/8H 80p 60q
Mode_5	640x480 Y (Mono) 8bit/pixel	16)16H 10240p 2560q	8)8H 5120p 1280q	4) 4H 2560p 640q	2) 2H 1280p 320q	1H 640p 160q	1/2H 320p 80q	1/4H 160p 40q	1/8H 80p 20q
Mode_6	640x480 Y (Mono16) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4) 2H 1280p 640q	2) 1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
Mode_7	Reserved								

Format_1

Mode	Video Format	240fps	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
Mode_0	800x600 YUV(4:2:2) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H 4000p 2000q	4) 5/2H 2000p 1000q	2) 5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
Mode_1	800x600 RGB 24bit/pixel		32)10H 8000p 6000q	16)5H 4000p 3000q	8)5/2H 2000p 1500q	4) 5/4H 1000p 750q	2) 5/8H 500p 375q		
Mode_2	800x600 Y (Mono) 8bit/pixel	16)20H 16000p 4000q	8)10H 8000p 2000q	4) 5H 4000p 1000q	2) 5/2H 2000p 500q	5/4H 1000p 250q	5/8H 500p 125q		
Mode_3	1024x768 YUV(4:2:2) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4) 3/2H 1536p 768q	2) 3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q
Mode_4	1024x768 RGB 24bit/pixel			32)6H 6144p 4608q	16)3H 3072p 2304q	8)3/2H 1536p 1152q	4) 3/4H 768p 576q	2) 3/8H 384p 288q	3/16H 192p 144q
Mode_5	1024x768 Y (Mono) 8bit/pixel	32)24H 24576p 6144q	16)12H 12288p 3072q	8)6H 6144p 1536q	4) 3H 3072p 768q	2) 3/2H 1536p 384q	3/4H 768p 192q	3/8H 384p 96q	3/16H 192p 48q
Mode_6	800x600 Y (Mono16) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H 4000p 2000q	4) 5/2H 2000p 1000q	2) 5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	

Mode_7	1024x768 Y (Mono16) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4) 3/2H 1536p 768q	2) 3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q

Format_2

Mode	Video Format	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
Mode_0	1280x960 YUV(4:2:2) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4) 1H 1280p 640q	2) 1/2H 640p 320q	1/4H 320p 160q
Mode_1	1280x960 RGB 24bit/pixel		32)8H 10240p 7680q	16)4H 5120p 3840q	8)2H 2560p 1920q	4) 1H 1280p 960q	2) 1/2H 640p 480q	1/4H 320p 240q
Mode_2	1280x960 Y (Mono) 8bit/pixel	32)16H 20480p 5120q	16)8H 10240p 2560q	8)4H 5120p 1280q	4) 2H 2560p 640q	2) 1H 1280p 320q	1/2H 640p 160q	1/4H 320p 80q
Mode_3	1600x1200 YUV(4:2:2) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000q	8)5/2H 4000p 2000q	4) 5/4H 2000p 1000q	2) 5/8H 1000p 500q	5/16H 500p 250q
Mode_4	1600x1200 RGB 24bit/pixel			32)5H 8000p 6000q	16)5/2H 4000p 3000q	8)5/4H 2000p 1500q	4) 5/8H 1000p 750q	2) 5/16H 500p 375q
Mode_5	1600x1200 Y (Mono) 8bit/pixel	32)20H 32000p 8000q	16)10H 16000p 4000q	8)5H 8000p 2000q	4) 5/2H 4000p 1000q	2) 5/4H 2000p 500q	5/8H 1000p 250q	5/16H 500p 125q
Mode_6	1280x960 Y (Mono16) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4) 1H 1280p 640q	2) 1/2H 640p 320q	1/4H 320p 160q
Mode_7	1600x1200 Y (Mono16) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000q	8)5/2H 4000p 2000q	4) 5/4H 2000p 1000q	2) 5/8H 1000p 500q	5/16H 500p 250q

[---H : Line / Packet] [---p : Pixel / Packet] [---q : Quadlet / Packet]

2) : required S200 data rate

4) : required S400 data rate

8) : required S800 data rate

16): required S1600 data rate

32): required S3200 data rate

5.1.3 Video data payload structure

Pn : Pixel number / packet

K : $Pn \times n$ (n = 0..N-1)

($Pn \times N$ = Total pixel number / frame.)

<YUV (4: 4: 4) format >

U-(K+0)	Y-(K+0)	V-(K+0)	U-(K+1)
Y-(K+1)	V-(K+1)	U-(K+2)	Y-(K+2)
V-(K+2)	U-(K+3)	Y-(K+3)	V-(K+3)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	U-(K+Pn-3)
Y-(K+Pn-3)	V-(K+Pn-3)	U-(K+Pn-2)	Y-(K+Pn-2)
V-(K+Pn-2)	U-(K+Pn-1)	Y-(K+Pn-1)	V-(K+Pn-1)

<YUV (4: 2: 2) format >

U-(K+0)	Y-(K+0)	V-(K+0)	Y-(K+1)
U-(K+2)	Y-(K+2)	V-(K+2)	Y-(K+3)
U-(K+4)	Y-(K+4)	V-(K+4)	Y-(K+5)
U-(K+Pn-6)	Y-(K+Pn-6)	V-(K+Pn-6)	Y-(K+Pn-5)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	Y-(K+Pn-3)
U-(K+Pn-2)	Y-(K+Pn-2)	V-(K+Pn-2)	Y-(K+Pn-1)

<YUV (4: 1: 1) format >

U-(K+0)	Y-(K+0)	Y-(K+1)	V-(K+0)
Y-(K+2)	Y-(K+3)	U-(K+4)	Y-(K+4)
Y-(K+5)	V-(K+4)	Y-(K+6)	Y-(K+7)
U-(K+Pn-8)	Y-(K+Pn-8)	Y-(K+Pn-7)	V-(K+Pn-8)
Y-(K+Pn-6)	Y-(K+Pn-5)	U-(K+Pn-4)	Y-(K+Pn-4)
Y-(K+Pn-3)	V-(K+Pn-4)	Y-(K+Pn-2)	Y-(K+Pn-1)

<RGB format >

R-(K+0)	G-(K+0)	B-(K+0)	R-(K+1)
G-(K+1)	B-(K+1)	R-(K+2)	G-(K+2)
B-(K+2)	R-(K+3)	G-(K+3)	B-(K+3)
R-(K+Pn-4)	G-(K+Pn-4)	B-(K+Pn-4)	R-(K+Pn-3)
G-(K+Pn-3)	B-(K+Pn-3)	R-(K+Pn-2)	G-(K+Pn-2)
B-(K+Pn-2)	R-(K+Pn-1)	G-(K+Pn-1)	B-(K+Pn-1)

<Y (Mono) format >

Y-(K+0)	Y-(K+1)	Y-(K+2)	Y-(K+3)
Y-(K+4)	Y-(K+5)	Y-(K+6)	Y-(K+7)
Y-(K+Pn-8)	Y-(K+Pn-7)	Y-(K+Pn-6)	Y-(K+Pn-5)
Y-(K+Pn-4)	Y-(K+Pn-3)	Y-(K+Pn-2)	Y-(K+Pn-1)

< Y (Mono16) format >

Y component has 16bit data.

High byte	Low byte

Y-(K+0)	Y-(K+1)
Y-(K+2)	Y-(K+3)
Y-(K+Pn-4)	Y-(K+Pn-3)
Y-(K+Pn-2)	Y-(K+Pn-1)

5.1.4 Little_Endian Mode

If Little_Endian mode is set, the order of the high and low bytes for the **< Y (Mono16) >** format shall be reversed as shown below.

Low byte	High byte

All other formats are not affected.

5.1.5 Data structure

<Y, R, G, B>

Each component has 8bit data. The data type is "Unsigned Char".

	Signal level (Decimal)	Data (Hexadecimal)
Highest	255	0xFF
	254	0xFE
	:	:
	1	0x01
Lowest	0	0x00

<U, V>

Each component has 8bit data. The data type is "Straight Binary".

	Signal level (Decimal)	Data (Hexadecimal)
Highest (+)	127	0xFF
	126	0xFE
	:	:
	1	0x81
Lowest	0	0x80
	-1	0x7F
	:	:
	-127	0x01
Highest (-)	-128	0x00

< Y(Mono16) >

Y component has 16bit data. The data type is "Unsigned Short (big-endian)".

Y	Signal level (Decimal)	Data (Hexadecimal)
Highest	65535	0xFFFF
	65534	0xFFFE
	:	:
	1	0x0001
Lowest	0	0x0000

5.2 Isochronous packet format for Partial image size video format (Format_7)

5.2.1 Video Isochronous packet structure

The following table shows the format of the first quadlet in the data field of each Isochronous data block.

0-7	8-15	16-23		24-31	
data_length		tg	channel	tCode	sy
header_CRC					
Video data payload					
data_CRC					

Isochronous Data Block Packet Format

Where the following fields are defined in the IEEE 1394 standard:

data_length : number of bytes in the data field

tg : (tag field) shall be set to zero

channel : isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register

tCode : (transaction code) shall be set to the isochronous data block packet tCode

sy : (synchronization value) shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous data blocks

Video data payload: shall contain the digital video information, as defined in the following sections.

5.2.2 Video data payload structure

Pn : Pixel number / packet

K : $Pn \times n$ (n = 0..N-1)

($Pn \times N$ = Total pixel number / frame.)

< Mono8 format (color coding ID = 0) >

Y component has 8bit data.

Y-(K+0)	Y-(K+1)	Y-(K+2)	Y-(K+3)
Y-(K+4)	Y-(K+5)	Y-(K+6)	Y-(K+7)
Y-(K+Pn-8)	Y-(K+Pn-7)	Y-(K+Pn-6)	Y-(K+Pn-5)
Y-(K+Pn-4)	Y-(K+Pn-3)	Y-(K+Pn-2)	Y-(K+Pn-1)

< 4:1:1 YUV8 format (color coding ID = 1)>

Each component has 8bit data.

U-(K+0)	Y-(K+0)	Y-(K+1)	V-(K+0)
Y-(K+2)	Y-(K+3)	U-(K+4)	Y-(K+4)
Y-(K+5)	V-(K+4)	Y-(K+6)	Y-(K+7)
U-(K+Pn-8)	Y-(K+Pn-8)	Y-(K+Pn-7)	V-(K+Pn-8)
Y-(K+Pn-6)	Y-(K+Pn-5)	U-(K+Pn-4)	Y-(K+Pn-4)
Y-(K+Pn-3)	V-(K+Pn-4)	Y-(K+Pn-2)	Y-(K+Pn-1)

< 4:2:2 YUV8 format (color coding ID = 2) >

Each component has 8bit data.

U-(K+0)	Y-(K+0)	V-(K+0)	Y-(K+1)
U-(K+2)	Y-(K+2)	V-(K+2)	Y-(K+3)
U-(K+4)	Y-(K+4)	V-(K+4)	Y-(K+5)
U-(K+Pn-6)	Y-(K+Pn-6)	V-(K+Pn-6)	Y-(K+Pn-5)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	Y-(K+Pn-3)
U-(K+Pn-2)	Y-(K+Pn-2)	V-(K+Pn-2)	Y-(K+Pn-1)

< 4:4:4 YUV8 format (color coding ID = 3) >

Each component has 8bit data.

U-(K+0)	Y-(K+0)	V-(K+0)	U-(K+1)
Y-(K+1)	V-(K+1)	U-(K+2)	Y-(K+2)
V-(K+2)	U-(K+3)	Y-(K+3)	V-(K+3)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	U-(K+Pn-3)
Y-(K+Pn-3)	V-(K+Pn-3)	U-(K+Pn-2)	Y-(K+Pn-2)
V-(K+Pn-2)	U-(K+Pn-1)	Y-(K+Pn-1)	V-(K+Pn-1)

<RGB8 format (color coding ID = 4) >

Each component has 8bit data.

R-(K+0)	G-(K+0)	B-(K+0)	R-(K+1)
G-(K+1)	B-(K+1)	R-(K+2)	G-(K+2)
B-(K+2)	R-(K+3)	G-(K+3)	B-(K+3)
R-(K+Pn-4)	G-(K+Pn-4)	B-(K+Pn-4)	R-(K+Pn-3)
G-(K+Pn-3)	B-(K+Pn-3)	R-(K+Pn-2)	G-(K+Pn-2)
B-(K+Pn-2)	R-(K+Pn-1)	G-(K+Pn-1)	B-(K+Pn-1)

< Mono16 format (color coding ID = 5) >

Y component has 16bit data.

High byte	Low byte

Y-(K+0)	Y-(K+1)
Y-(K+2)	Y-(K+3)
Y-(K+Pn-4)	Y-(K+Pn-3)
Y-(K+Pn-2)	Y-(K+Pn-1)

< RGB16 format (color coding ID = 6) >

Each component has 16bit data.

High byte	Low byte

R-(K+0)	G-(K+0)
B-(K+0)	R-(K+1)
G-(K+1)	B-(K+1)
B-(K+Pn-2)	R-(K+Pn-1)
G-(K+Pn-1)	B-(K+Pn-1)

< Signed Mono16 format (color coding ID = 7) >

Y component has 16bit signed integer data.

High byte	Low byte

Y-(K+0)	Y-(K+1)
Y-(K+2)	Y-(K+3)
Y-(K+Pn-4)	Y-(K+Pn-3)
Y-(K+Pn-2)	Y-(K+Pn-1)

< Signed RGB16 format (color coding ID = 8) >

Each component has 16bit signed integer data.

High byte	Low byte

R-(K+0)	G-(K+0)
B-(K+0)	R-(K+1)
G-(K+1)	B-(K+1)
B-(K+Pn-2)	R-(K+Pn-1)
G-(K+Pn-1)	B-(K+Pn-1)

<Raw data8 (Bayer Arrangement Primary Color Filter) format (color coding ID=9)>

Each component has 8bit data.

W : Image width (pixel)

K : W * n (n = 0..N-1)

<Filter ID = 0 (RG/GB)>

Even line

R-(K+0)	Gr-(K+1)	R-(K+2)	Gr-(K+3)
R-(K+4)	Gr-(K+5)	R-(K+6)	Gr-(K+7)
R-(K+W-8)	Gr-(K+W-7)	R-(K+W-6)	Gr-(K+W-5)
R-(K+W-4)	Gr-(K+W-3)	R-(K+W-2)	Gr-(K+W-1)

Odd line

Gb-(K+0)	B-(K+1)	Gb-(K+2)	B-(K+3)
Gb-(K+4)	B-(K+5)	Gb-(K+6)	B-(K+7)
Gb-(K+W-8)	B-(K+W-7)	Gb-(K+W-6)	B-(K+W-5)
Gb-(K+W-4)	B-(K+W-3)	Gb-(K+W-2)	B-(K+W-1)

<Filter ID = 1 (GB/RG)>

Even line

Gb-(K+0)	B-(K+1)	Gb-(K+2)	B-(K+3)
Gb-(K+4)	B-(K+5)	Gb-(K+6)	B-(K+7)
Gb-(K+W-8)	B-(K+W-7)	Gb-(K+W-6)	B-(K+W-5)
Gb-(K+W-4)	B-(K+W-3)	Gb-(K+W-2)	B-(K+W-1)

Odd line

R-(K+0)	Gr-(K+1)	R-(K+2)	Gr-(K+3)
R-(K+4)	Gr-(K+5)	R-(K+6)	Gr-(K+7)
R-(K+W-8)	Gr-(K+W-7)	R-(K+W-6)	Gr-(K+W-5)
R-(K+W-4)	Gr-(K+W-3)	R-(K+W-2)	Gr-(K+W-1)

<Filter ID = 2 (GR/BG)>

Even line

Gr-(K+0)	R-(K+1)	Gr-(K+2)	R-(K+3)
Gr-(K+4)	R-(K+5)	Gr-(K+6)	R-(K+7)
Gr-(K+W-8)	R-(K+W-7)	Gr-(K+W-6)	R-(K+W-5)
Gr-(K+W-4)	R-(K+W-3)	Gr-(K+W-2)	R-(K+W-1)

Odd line

B-(K+0)	Gb-(K+1)	B-(K+2)	Gb-(K+3)
B-(K+4)	Gb-(K+5)	B-(K+6)	Gb-(K+7)
B-(K+W-8)	Gb-(K+W-7)	B-(K+W-6)	Gb-(K+W-5)
B-(K+W-4)	Gb-(K+W-3)	B-(K+W-2)	Gb-(K+W-1)

<Filter ID = 3 (BG/GR)>

Even line

B-(K+0)	Gb-(K+1)	B-(K+2)	Gb-(K+3)
B-(K+4)	Gb-(K+5)	B-(K+6)	Gb-(K+7)
B-(K+W-8)	Gb-(K+W-7)	B-(K+W-6)	Gb-(K+W-5)
B-(K+W-4)	Gb-(K+W-3)	B-(K+W-2)	Gb-(K+W-1)

Odd line

Gr-(K+0)	R-(K+1)	Gr-(K+2)	R-(K+3)
Gr-(K+4)	R-(K+5)	Gr-(K+6)	R-(K+7)
Gr-(K+W-8)	R-(K+W-7)	Gr-(K+W-6)	R-(K+W-5)
Gr-(K+W-4)	R-(K+W-3)	Gr-(K+W-2)	R-(K+W-1)

<Raw data16 (Bayer Arrangement Primary Color Filter) format (color coding ID=10)>

Each component has 16bit data.

W : Image width (pixel)

K : W * n (n = 0..N-1)

High byte	Low byte

<Filter ID = 0 (RG/GB)>

Even line

R-(K+0)	Gr-(K+1)
R-(K+2)	Gr-(K+3)
R-(K+W-4)	Gr-(K+W-3)
R-(K+W-2)	Gr-(K+W-1)

Odd line

Gb-(K+0)	B-(K+1)
Gb-(K+2)	B-(K+3)
Gb-(K+W-4)	B-(K+W-3)
Gb-(K+W-2)	B-(K+W-1)

<Filter ID = 1 (GB/RG)>

Even line

R-(K+0)	Gr-(K+1)
R-(K+2)	Gr-(K+3)
R-(K+W-4)	Gr-(K+W-3)
R-(K+W-2)	Gr-(K+W-1)

Odd line

Gb-(K+0)	B-(K+1)
Gb-(K+2)	B-(K+3)
Gb-(K+W-4)	B-(K+W-3)
Gb-(K+W-2)	B-(K+W-1)

<Filter ID = 2 (GR/BG)>

Even line

Gr-(K+0)	R-(K+1)
Gr -(K+2)	R-(K+3)
Gr -(K+W-4)	R-(K+W-3)
Gr -(K+W-2)	R-(K+W-1)

Odd line

B-(K+0)	Gb-(K+1)
B-(K+2)	Gb-(K+3)
B-(K+W-4)	Gb-(K+W-3)
B-(K+W-2)	Gb-(K+W-1)

<Filter ID = 3 (BG/GR)>

Even line

B-(K+0)	Gb-(K+1)
B-(K+2)	Gb-(K+3)
B-(K+W-4)	Gb-(K+W-3)
B-(K+W-2)	Gb-(K+W-1)

Odd line

Gr-(K+0)	R-(K+1)
Gr -(K+2)	R-(K+3)
Gr -(K+W-4)	R-(K+W-3)
Gr -(K+W-2)	R-(K+W-1)

< Mono12 format (color coding ID = 11) >

Y component has 12bit data.

High byte	Low nibble

Y-(K+0) High byte		Y-(K+1) Low nibble	Y-(K+0) Low nibble	Y-(K+1) High byte		Y-(K+2) High byte	
Y-(K+3) Low nibble	Y-(K+2) Low nibble	Y-(K+3) High byte		Y-(K+4) High byte		Y-(K+5) Low nibble	Y-(K+4) Low nibble
Y-(K+Pn-5) Low nibble	Y-(K+Pn-6) Low nibble	Y-(K+Pn-5) High byte		Y-(K+Pn-4) High byte		Y-(K+Pn-3) Low nibble	Y-(K+Pn-4) Low nibble
Y-(K+Pn-3) High byte		Y-(K+Pn-2) High byte		Y-(K+Pn-1) Low nibble	Y-(K+Pn-2) Low nibble	Y-(K+Pn-1) High byte	

<Raw data12 (Bayer Arrangement Primary Color Filter) format (color coding ID=12)>

Each component has 12bit data.

W : Image width (pixel)

K : W * n (n = 0..N-1)

High byte	Low nibble

<Filter ID = 0 (RG/GB)>

Even line

R-(K+0) High byte		Gr-(K+1) Low nibble	R-(K+0) Low nibble	Gr-(K+1) High byte		R-(K+2) High byte	
Gr-(K+3) Low nibble	R-(K+2) Low nibble	Gr-(K+3) High byte		R-(K+4) High byte		Gr-(K+5) Low nibble	R-(K+4) Low nibble
Gr-(K+W-5) Low nibble	R-(K+W-6) Low nibble	Gr-(K+W-5) High byte		R-(K+W-4) High byte		Gr-(K+W-3) Low nibble	R-(K+W-4) Low nibble
Gr-(K+W-3) High byte		R-(K+W-2) High byte		Gr-(K+W-1) Low nibble	R-(K+W-2) Low nibble	Gr-(K+W-1) High byte	

Odd line

Gb-(K+0) High byte		B-(K+1) Low nibble	Gb-(K+0) Low nibble	B-(K+1) High byte		Gb -(K+2) High byte	
B-(K+3) Low nibble	Gb -(K+2) Low nibble	B-(K+3) High byte		Gb -(K+4) High byte		B-(K+5) Low nibble	Gb -(K+4) Low nibble

B-(K+W-5) Low nibble	Gb-(K+W-6) Low nibble	B-(K+W-5) High byte	Gb-(K+W-4) High byte	B-(K+W-3) Low nibble	Gb-(K+W-4) Low nibble
B-(K+W-3) High byte		Gb-(K+W-2) High byte	B-(K+W-1) Low nibble	Gb-(K+W-2) Low nibble	B-(K+W-1) High byte

<Filter ID = 1 (GB/RG)>

Even line

Gb-(K+0) High byte		B-(K+1) Low nibble	Gb-(K+0) Low nibble	B-(K+1) High byte	Gb-(K+2) High byte
B-(K+3) Low nibble	Gb -(K+2) Low nibble	B-(K+3) High byte		Gb-(K+4) High byte	B-(K+5) Low nibble	Gb-(K+4) Low nibble
B-(K+W-5) Low nibble	Gb-(K+W-6) Low nibble	B-(K+W-5) High byte		Gb -(K+W-4) High byte	B-(K+W-3) Low nibble	Gb-(K+W-4) Low nibble
B-(K+W-3) High byte		Gb -(K+W-2) High byte	B-(K+W-1) Low nibble	Gb-(K+W-2) Low nibble	B-(K+W-1) High byte

Odd line

R-(K+0) High byte		Gr-(K+1) Low nibble	R-(K+0) Low nibble	Gr-(K+1) High byte	R-(K+2) High byte
Gr -(K+3) Low nibble	R-(K+2) Low nibble	Gr-(K+3) High byte		R -(K+4) High byte	Gr-(K+5) Low nibble	R-(K+4) Low nibble
Gr -(K+W-5) Low nibble	R-(K+W-6) Low nibble	Gr -(K+W-5) High byte		R-(K+W-4) High byte	Gr -(K+W-3) Low nibble	R-(K+W-4) Low nibble
Gr -(K+W-3) High byte		R-(K+W-2) High byte	Gr -(K+W-1) Low nibble	R-(K+W-2) Low nibble	Gr -(K+W-1) High byte

<Filter ID = 2 (GR/BG)>

Even line

Gr-(K+0) High byte		R-(K+1) Low nibble	Gr-(K+0) Low nibble	R-(K+1) High byte	Gr R-(K+2) High byte
R-(K+3) Low nibble	Gr-(K+2) Low nibble	R-(K+3) High byte		R-(K+4) High byte	R-(K+5) Low nibble	Gr-(K+4) Low nibble
R-(K+W-5) Low nibble	Gr-(K+W-6) Low nibble	R-(K+W-5) High byte		Gr-(K+W-4) High byte	R-(K+W-3) Low nibble	Gr-(K+W-4) Low nibble
R-(K+W-3) High byte		Gr-(K+W-2) High byte	R-(K+W-1) Low nibble	Gr-(K+W-2) Low nibble	R-(K+W-1) High byte

Odd line

B-(K+0) High byte		Gb-(K+1) Low nibble	B-(K+0) Low nibble	Gb-(K+1) High byte		B-(K+2) High byte	
Gb-(K+3) Low nibble	B -(K+2) Low nibble	Gb-(K+3) High byte		B -(K+4) High byte		Gb-(K+5) Low nibble	B -(K+4) Low nibble
Gb-(K+W-5) Low nibble	B-(K+W-6) Low nibble	Gb-(K+W-5) High byte		B-(K+W-4) High byte		Gb-(K+W-3) Low nibble	B-(K+W-4) Low nibble
Gb-(K+W-3) High byte		B-(K+W-2) High byte		Gb-(K+W-1) Low nibble	B-(K+W-2) Low nibble	Gb-(K+W-1) High byte	

<Filter ID = 3 (BG/GR)>

Even line

B-(K+0) High byte		Gb-(K+1) Low nibble	B-(K+0) Low nibble	Gb-(K+1) High byte		B-(K+2) High byte	
Gb-(K+3) Low nibble	B-(K+2) Low nibble	Gb-(K+3) High byte		B-(K+4) High byte		Gb-(K+5) Low nibble	B-(K+4) Low nibble
Gb-(K+W-5) Low nibble	B-(K+W-6) Low nibble	Gb-(K+W-5) High byte		B-(K+W-4) High byte		Gb-(K+W-3) Low nibble	B-(K+W-4) Low nibble
Gb-(K+W-3) High byte		B-(K+W-2) High byte		Gb-(K+W-1) Low nibble	B-(K+W-2) Low nibble	Gb-(K+W-1) High byte	

Odd line

GR-(K+0) High byte		R-(K+1) Low nibble	Gr-(K+0) Low nibble	R-(K+1) High byte		Gr -(K+2) High byte	
R-(K+3) Low nibble	Gr -(K+2) Low nibble	r-(K+3) High byte		Gr -(K+4) High byte		R-(K+5) Low nibble	Gr -(K+4) Low nibble
R-(K+W-5) Low nibble	Gr-(K+W-6) Low nibble	R-(K+W-5) High byte		Gr-(K+W-4) High byte		R-(K+W-3) Low nibble	Gr-(K+W-4) Low nibble
R-(K+W-3) High byte		Gr-(K+W-2) High byte		R-(K+W-1) Low nibble	Gr-(K+W-2) Low nibble	R-(K+W-1) High byte	

5.2.3 Little_Endian Mode

If Little_Endian mode is set, the order of the high and low bytes for <**Mono16, RGB16, Signed Mono16, Signed RGB16, Raw data16**> formats shall be reversed as shown below.

Low byte	High byte

All other formats are not affected.

5.2.4 Data structure

< Mono8, RGB8 >

Each component (Y, R, G, B) has 8bit data. The data type is “Unsigned Char”.

Y,R,G,B	Signal level (Decimal)	Data (Hexadecimal)
Highest	255	0xFF
	254	0xFE
	:	:
	1	0x01
Lowest	0	0x00

< YUV8 >

Each component (Y, U, V) has 8bit data. The Y component is the same as in the above table. The data type is "Straight Binary" for U and V data.

U, V	Signal level (Decimal)	Data (Hexadecimal)
Highest (+)	127	0xFF
	126	0xFE
	:	:
	1	0x81
Lowest	0	0x80
	-1	0x7F
	:	:
	-127	0x01
Highest (-)	-128	0x00

< Mono16, RGB16 >

Each component (Y,R,G,B) has 16bit data. The data type is “Unsigned Short (big-endian)”.

Y,R,G,B	Signal level (Decimal)	Data (Hexadecimal)
Highest	65535	0xFFFF
	65534	0xFFFE
	:	:
	1	0x0001
Lowest	0	0x0000

< Signed Mono16, RGB16 >

Each component (Y,R,G,B) has signed 16bit data. The data type is “Signed Short (big-endian)”.

Y,R,G,B	Signal level (Decimal)	Data (Hexadecimal)
Highest	32767	0x7FFF
	32766	0x7FFE
	:	:
	1	0x0001
	0	0x0000
	-1	0xFFFF
	:	:
	-32767	0x8001
Lowest	-32768	0x8000

< Mono12 >

Each component (Y) has 12bit data. The data type is “Unsigned Short (big-endian)”.

Y	Signal level (Decimal)	Data (Hexadecimal)
Highest	4095	0xFFF
	4094	0xFFE
	:	:
	1	0x001
Lowest	0	0x000

6 Serial bus management

This chapter describes the camera behavior on a given Serial Bus. (IEEE 1394 Digital Camera is in accordance with IEEE standard 1212-1991.)

6.1 Bus Management

The camera compliant with this specification is a peripheral for a personal computer or workstation. Another node on the IEEE 1394 bus, such as a computer, acts as the camera controller.

In order for the camera to perform any action, the camera controller shall access the camera control registers, as described in this standard.

The camera is neither Isochronous manager capable nor full bus manager capable. The camera is also not cycle master capable. The contents of the self_ID packet generated by the camera, and the contents of camera configuration ROM shall accurately reflect this level of capability.

In order for the camera to perform any action, it shall be connected to other IEEE 1394 nodes. At a minimum, there shall be a cycle master capable node and an Isochronous manager capable node. In addition, there shall be some node that is running application software that implements the protocol described in this standard. Note that all of these capabilities could reside in a single node.

The camera controller is responsible for the following activities related to camera operation:

- Force a cycle master capable node to be the root
- Start cycle master operation
- Initialize the camera control registers for a desired video mode, frame rate, etc.
- Allocate Isochronous resources needed by the camera (Isochronous channel number and bandwidth, as needed for the selected video mode)
- Program the Isochronous channel number and transmit speed into the camera control registers
- Instruct the camera to start sourcing Isochronous video data
- The camera continues sourcing Isochronous video data until the camera controller instructs the camera to stop. If a bus reset occurs during camera operation, the camera continues sourcing Isochronous data immediately after the bus reset.

6.2 Asynchronous Transfer Capabilities

The camera compliant with this specification shall be capable of sending and receiving the asynchronous packets with a payload of up to the maximum payload size of “mac_rec” field of the Configuration ROM.

6.3 Isochronous Transfer Capabilities

The camera compliant with this specification is capable of being an Isochronous talker. The camera is not capable of listening to a channel of Isochronous data.

6.4 IEEE 1394 Specific Address Space

The camera compliant with this specification shall be compliant with the IEEE 1394 and IEEE 1212 standards.

The following sections define all CSR and ROM locations that the camera shall implement. All information in these sections is intended to comply with the IEEE 1394 standard. Where discrepancies arise, the IEEE 1394 standard shall prevail.

All address-offset locations in these sections are with respect to a base address of:

FFFF F000 0000h

6.4.1 Implemented CSR's

The digital camera implements the following core CSR's, as required by the IEEE 1394 standard:

Offset	0-7	8-15	16-23	24-31
0000h	STATE_CLEAR			
0004h	STATE_SET			
0008h	NODE_IDS			
000Ch	RESET_START			
0010h				
0014h				
0018h	SPLIT_TIMEOUT_HI			
001Ch	SPLIT_TIMEOUT_LO			

Core CSR's

The digital camera implements the following IEEE 1394 Serial Bus dependent CSR's:

Offset	0-7	8-15	16-23	24-31
0200h	CYCLE_TIME			
0204h				
0208h				
020Ch				
0210h	BUSY_TIMEOUT			

Serial Bus Dependent CSR's

6.4.2 Configuration ROM

IEEE 1394 Digital Camera implements the Configuration ROM as defined in IEEE standard 1212-1991, IEEE standard 1394-2008. These assignments are only an example. Key code can describe the roll of registers so some of registers' order is not mandatory. Please see IEEE std 1212 specification in detail.

unit_sw_version = 0x000102 (for 1394 based Digital Camera specification version 1.30)

History:

- unit_sw_version = 0x000101 (for 1394 based Digital Camera specification version 1.20)

- unit_sw_version = 0x000100 (for 1394 based Digital Camera specification version 1.04)

	Offset	0-7	8-15	16-23	24-31
Bus Info Block	400h	04h	crc_length	rom_crc_value	
	404h	31h	33h	39h	34h
	408h	0 0 1 0 R	FFh	max_rec | r | mxrom	gen | r | Lk_spd
	40Ch	node_vendor_id			chip_id_hi
	410h	chip_id_lo			
Root Directory	414h	0004h		CRC	
	418h	03h	module_vendor_ID		
	41Ch	0Ch	Reserved	1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0	
	420h	8Dh	indirect_offset (only valid for IEEE Std1394-1995 compliant camera)		
	424h	D1h	unit_directory offset		

Root Directory

The abbreviations of "r, mxrom, gen and link_spd" in the above table mean the "reserved, max_ROM, generation and link_spd" defined in the IEEE Std 1394-2008.

	Offset	0-7	8-15	16-23	24-31
Node unique ID leaf	0000h	0002h		CRC	
	0004h	node_vendor_id			chip_id_hi
	0008h	chip_id_lo			

Node Unique ID leaf

Node_Unique_ID leaf is removed from IEEE Std 1394a-2000. This leaf should be implemented only for IEEE Std 1394-1995 compliant camera.

	Offset	0-7	8-15	16-23	24-31
Unit Directory	0000h	0003h		CRC	
	0004h	12h	unit_spec_ID (=0x00A02D)		
	0008h	13h	unit_sw_version (=0x000102)		
	000Ch	D4h	unit_dependent_directory offset		

Unit directory

	Offset	0-7	8-15	16-23	24-31
Unit Dependent Info	0000h	unit_dep_info_length		CRC	
	0004h	40h	command_regs_base		
	0008h	81h	vendor_name_leaf		
	000Ch	82h	model_name_leaf		
	0010h	38h	unit_sub_sw_version		
	0014h	39h	Reserved		
	0018h	3Ah	Reserved		
	001Ch	3Bh	Reserved		
	0020h	3Ch	vendor_unique_info_0		
	0024h	3Dh	vendor_unique_info_1		
	0028h	3Eh	vendor_unique_info_2		
	002Ch	3Fh	vendor_unique_info_3		

Unit Dependent Directory

Where:

command_regs_base is the quadlet offset from the base address of initial register space of the base address of the command registers defined in section 1 of this standard.

vendor_name_leaf specifies the number of quadlets from the address of the vendor_name_leaf entry to the address of the vendor_name leaf containing an ASCII representation of the vendor name of this node.

model_name_leaf specifies the number of quadlets from the address of the model_name_leaf entry to the address of the model_name leaf containing an ASCII representation of the model name of this node.

Unit_sub_sw_version_info specifies the sub version information of this unit.

-unit_sub_sw_version = 0x000000h or unspecified for IIDC v1.30

-unit_sub_sw_version = 0x000010h for IIDC v1.31

-unit_sub_sw_version = 0x000020h for IIDC v1.32 (This Version)

:

-unit_sub_sw_version = 0x000090h for IIDC v1.39

Vendor_unique_info_x can specifies the vendor unique information, if need.

6.4.3 Format of Vendor Name and Model Name Leaves

The unit dependent directory may contain pointers to information leaves that contain the ASCII name of the vendor and model name for this node. The format of these leaves is shown in the following table:

	Offset	0-7	8-15	16-23	24-31
Name Leaf	0000h	leaf_length		CRC	
	0004h	00h	00 0000h		
	0008h	0000 0000h			
	000Ch	char_0	char_1	char_2	char_3
	0010h	char_4	char_5	char_6	char_7
	0014h	char_8	...		
	n+6h	...			char_n-3
	n+Ah	char_n-2	Char_n-1	NUL	NUL

Vendor Name/Model Name Leaves

Annex A
(informative)

Feature Definition and Specification

A.1 Brightness Control

Black level of the pictur

Off state:

Brightness level will be fixed value.

Auto control state:

Camera controls brightness level automatically by itself continuously.

Manual control state:

Camera controls brightness level manually by writing value to value-field.

One-Push action:

Camera controls brightness level automatically by itself only once and returns to Manual mode with adjusted value.

A.2 Auto Exposure Control

This feature is similar to "Contrast control".

Off state:

Exposure will be controlled manually using "Gain", "Iris" and/or "Shutter" features.

Auto control state:

Camera controls reference level automatically by itself continuously

Manual control state:

Camera controls exposure level automatically, but user can change reference level by writing value to "Auto_Exposure" register.

One-Push action:

Camera controls reference level automatically by itself only once and returns to Manual control state with adjusted value.

A.3 Sharpness Control

Sharpness of the picture.

Off state:

Sharpness level will be fixed value.

Auto control state:

Camera controls sharpness level automatically by itself continuously.

Manual control state:

Camera controls sharpness level manually by writing value to value-field.

One-Push action:

Camera controls sharpness level automatically by itself only once and returns to Manual control state with adjusted value.

A.4 White Balance Control

Adjustment of the white color of the picture.

At the YUV video mode, controlled by U value and V value.

At the RGB video mode, controlled by B value and R value.

Off state:

White balance will be fixed value.

Auto control state:

Camera controls white balance automatically by itself continuously.

Manual control state:

Camera controls white balance manually by writing value to value-field.

One-Push action:

Camera controls white balance automatically by itself only once and returns to Manual control state with adjusted value.

A.5 Hue Control

Color phase of the picture.

Off state:

Hue will be fixed value.

Auto control state:

Camera controls hue automatically by itself continuously.

Manual control state:

Camera controls hue manually by writing value to value-field.

One-Push action:

Camera controls hue automatically by itself only once and returns to Manual control state with adjusted value.

A.6 Saturation Control

Color saturation of the picture.

Off state:

Saturation level will be fixed value.

Auto control state:

Camera controls saturation level automatically by itself continuously.

Manual control state:

Camera controls saturation level manually by writing value to value-field.

One-Push action:

Camera controls saturation level automatically by itself only once and returns to Manual control state with adjusted value.

A.7 Gamma Control

Define the function between incoming light level and output picture level.

$$y = f(x)$$

y : output picture level x : incoming light level

Off state:

Gamma will be fixed value.

Auto control state:

Camera controls gamma automatically by itself continuously.

Manual control state:

Camera controls gamma manually by writing value to value-field.

One-Push action:

Camera controls gamma automatically by itself only once and returns to Manual control state with adjusted value.

A.8 Shutter Control

Integration time of the incoming light.

Off state:

Integration time will be fixed value.

Auto control state:

Camera controls integration time automatically by itself continuously.

Manual control state:

Camera controls integration time manually by writing value to value-field.

One-Push action:

Camera controls integration time automatically by itself only once and returns to Manual control state with adjusted value.

A.9 Gain Control

Camera circuits gain control.

Off state:

Gain level will be fixed value.

Auto control state:

Camera controls gain level automatically by itself continuously.

Manual control state:

Camera controls gain level manually by writing value to value-field.

One-Push action:

Camera controls gain level automatically by itself only once and returns to Manual control state with adjusted value.

A.10 Iris Control

Mechanical lens iris control.

Off state:

Iris will be fixed value.

Auto control state:

Camera controls iris automatically by itself continuously.

Manual control state:

Camera controls iris manually by writing value to value-field.

One-Push action:

Camera controls iris automatically by itself only once and returns to Manual control state with adjusted value.

A.11 Focus Control

Lens focus control.

Off state:

Focus will be fixed value.

Auto control state:

Camera controls focus automatically by itself continuously.

Manual control state:

Camera controls focus manually by writing value to value-field.

One-Push action:

Camera controls focus automatically by itself only once and returns to Manual control state with adjusted value.

A.12 Temperature Control

Getting the sensor temperature inside of the camera and/or controlling temperature.

Off state:

Camera stops temperature control.

Auto control state:

Camera controls temperature by itself aims to "Target_Temperature" continuously.

User can get temperature at the present time from "Temperature" value.

Manual control state:

In this mode, camera controls temperature by itself. But "Target_Temperature" value will be ignored. User can only get temperature at the present time from "Temperature" value.

One-Push action:

Camera controls temperature by itself aims to "Target_Temperature" value only once. User can get temperature at the present time from "Temperature" value.

A.13 Trigger Control

If this feature is turned on, trigger function will work.

Off state:

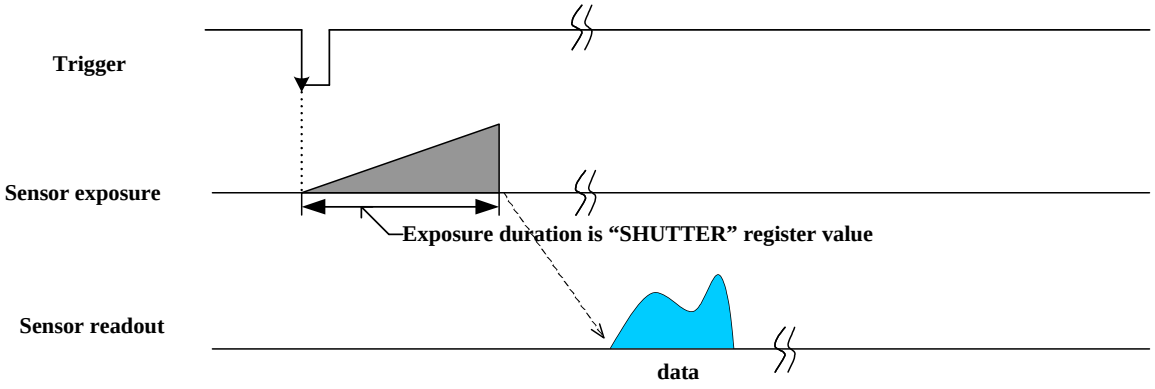
Trigger input is ignored.

Trigger mode definition

In the following explanation, trigger input is in case of “Low Active”. (Trigger_Polarity = 0)

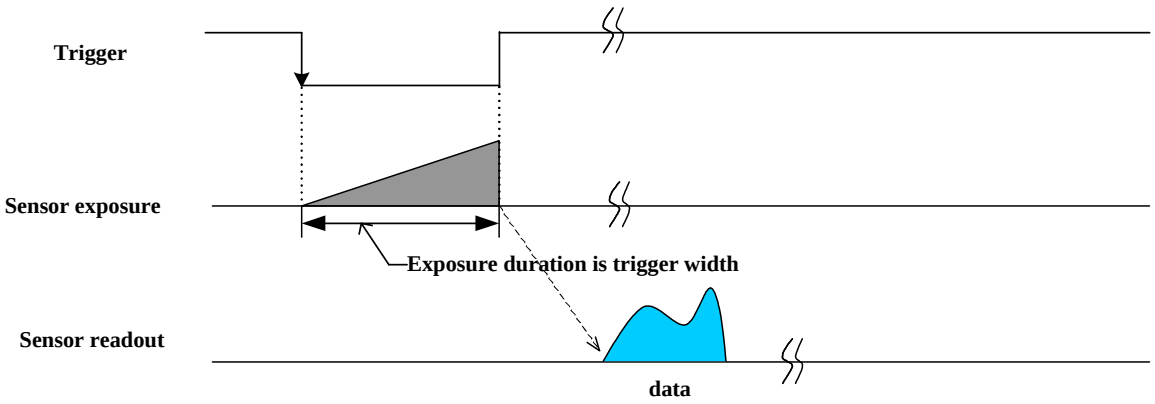
Trigger mode 0:

Camera starts integration of the incoming light from external trigger input falling edge. Integration time is described in "Shutter" register. No parameter is needed.



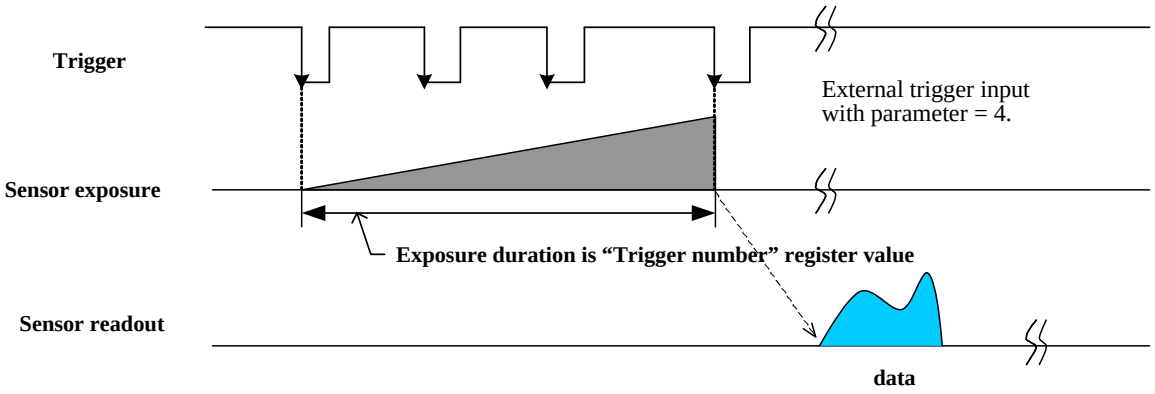
Trigger mode 1:

Camera starts integration of the incoming light from external trigger input falling edge. Integration time is equal to low state time of the external trigger input. No parameter is needed.



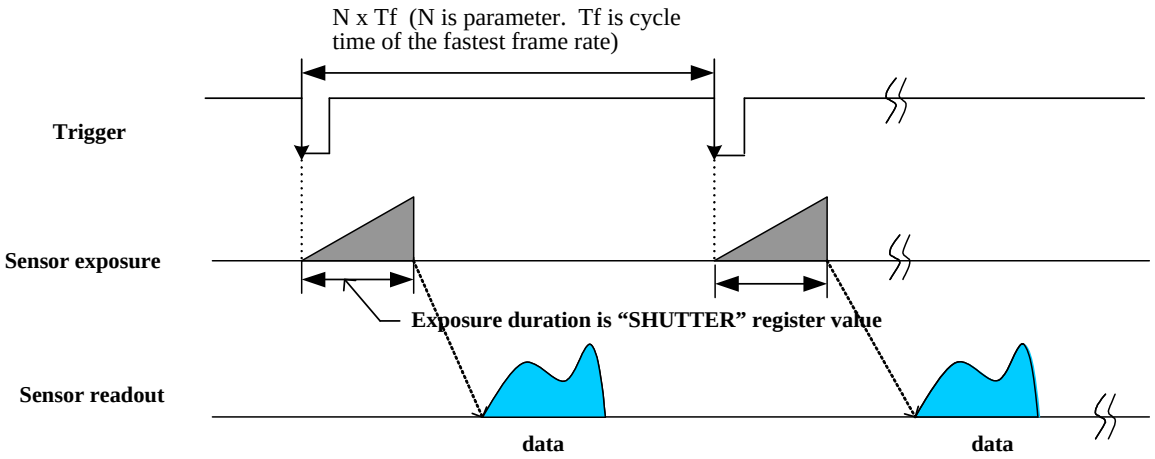
Trigger mode 2:

Camera starts integration of incoming light from first external trigger input falling edge. At the N-th (parameter) external trigger input falling edge, integration will be stopped. Parameter is required and shall be two or more. (N >= 2)



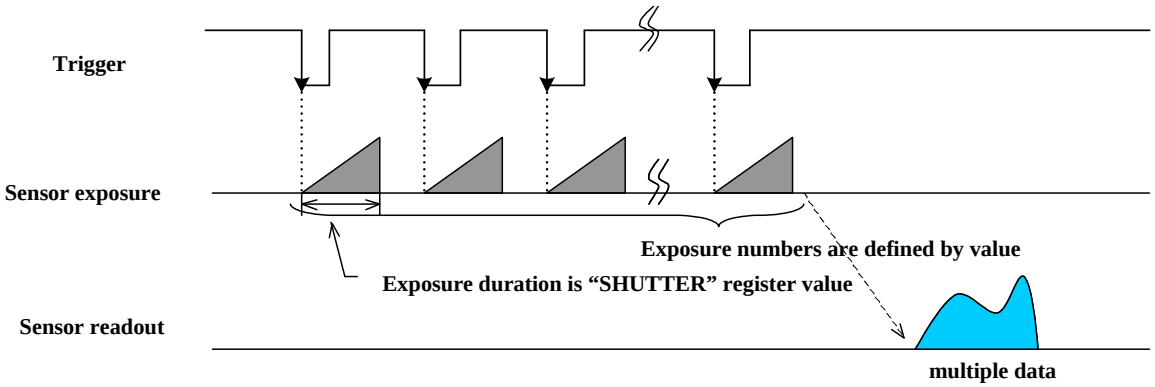
Trigger mode 3:

This is an internal trigger mode. Camera will issue trigger internally and cycle time is N times (parameter) of the cycle time of fastest frame rate. Integration time of incoming light is described in "Shutter" register. Parameter is required and shall be one or more. (N >= 1)



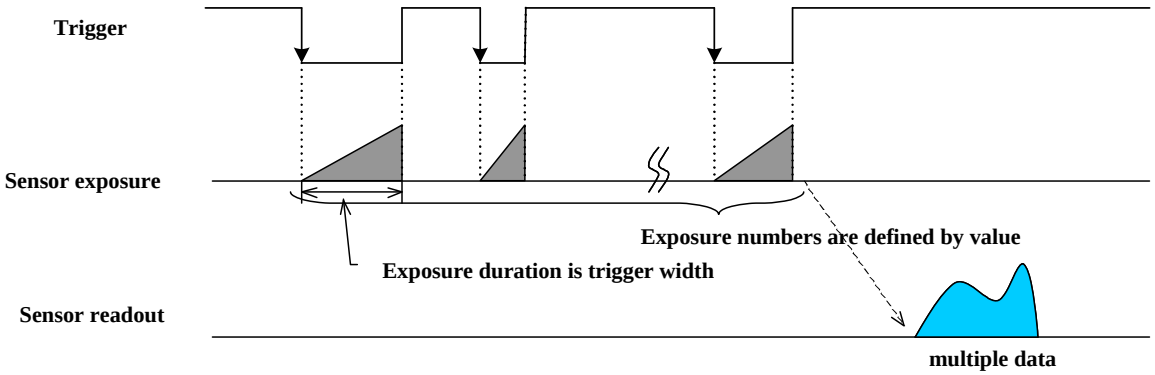
Trigger mode 4:

This mode is "multiple shutter preset mode". Camera starts integration of incoming light from first external trigger input falling edge and exposes incoming light at shutter time. Repeat this sequence the N-th (parameter) external trigger input falling edge then finish integration. Parameter is required and shall be one or more. (N >= 1)



Trigger mode 5:

This mode is "multiple shutter pulse width mode". Camera starts integration of incoming light from first external trigger input falling edge and exposes incoming light until trigger is inactive. Repeat this sequence the N-th (parameter) external trigger input falling edge then finish integration. Parameter is required and shall be one or more. (N >= 1)



Trigger mode 14,15:

These trigger modes are vendor unique. Camera vendor can implement vendor unique trigger mode here.

A.14 Trigger Delay Control

Add internal delay of trigger signal.

Off state:

No additional internal trigger delay.

A.15 White Shading Compensation

Adjust white shading compensation.

Off state:

White shading compensation level will be fixed value.

Auto control state:

Camera controls white shading compensation level automatically by itself continuously.

Manual control state:

Camera controls white shading compensation level by writing value to value-field.

One push action:

Camera controls white shading compensation level automatically by itself only once and returns to Manual control state with adjusted value.

Value explanation:

R_value:

Red channel compensation value. Write the value in AUTO mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning

G_value:

Green channel compensation value. Write the value in AUTO mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning

B_value:

Blue channel compensation value. Write the value in AUTO mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning

A.16 Frame Rate Prioritize Control

The frame interval is fixed by the frame rate value. When this feature is ON, exposure time is limited by frame rate value dynamically. The valid minimum and maximum shutter feature values should be checked when the frame rate is changed. If shutter (exposure) value is longer, it may be forced to change maximum value automatically. The available frame rate range depends on the current video format and/or video mode and the camera implementation. It is strongly recommended to check minimum and maximum value after video format and/or video mode have been changed.

Off state:

Frame interval is controlled by shutter value.

Auto control state:

Camera controls frame rate automatically by itself continuously.

Manual control state:

Camera controls frame interval based on frame rate value.

Example of usage:

Camera is in 640x480 Y8 mode at 30Hz (Cur_V_Frm_Rate=4)

Assume units of Value are 1/60000s (13.333us)

Frame_Rate_Inq:

Presence_Inq = 1

Abs_Ctrl_Inq = 0

One_Push_Inq = 0

On/Off_Inq = 1

ReadOut_Inq = 1

Auto_Inq = 0

Min_Value = 1875

Max_Value = 4000

Frame_Rate_Inq	On_Off	Value	Frame_Rate
800007D0h	0	2000	Depends on shutter time
82000753h	1	1875	32Hz
820007D0h	1	2000	30Hz
820007D2h	1	2002	29.97Hz(NTSC)
82000960h	1	2400	25Hz
82000EA6h	1	3750	16Hz
82000FA0h	1	4000	15Hz

A.17 Zoom Control

Lens zoom control.

Off state:

Zoom will be fixed value.

Auto control state:

Camera controls zoom automatically by itself continuously.

Manual control state:

Camera controls zoom manually by writing value to value-field.

One-Push action:

Camera controls zoom automatically by itself only once and returns to Manual control state with adjusted value.

A.18 Pan Control

Camera pan control.

Off state:

Pan will be fixed value.

Auto control state:

Camera controls pan automatically by itself continuously.

Manual control state:

Camera controls pan manually by writing value to value-field.

One-Push action:

Camera controls pan automatically by itself only once and returns to Manual control state with adjusted value.

A.19 Tilt Control

Camera tilt control.

Off state:

Tilt will be fixed value.

Auto control state:

Camera controls tilt automatically by itself continuously.

Manual control state:

Camera controls tilt manually by writing value to value-field.

One-Push action:

Camera controls tilt automatically by itself only once and returns to Manual control state with adjusted value.

A.20 Optical filter Control

Changing optical filter of camera lens function.

Off state:

Optical filter will be fixed value.

Auto control state:

Camera controls optical filter automatically by itself continuously.

Manual control state:

Camera controls optical filter manually by writing value to value-field.

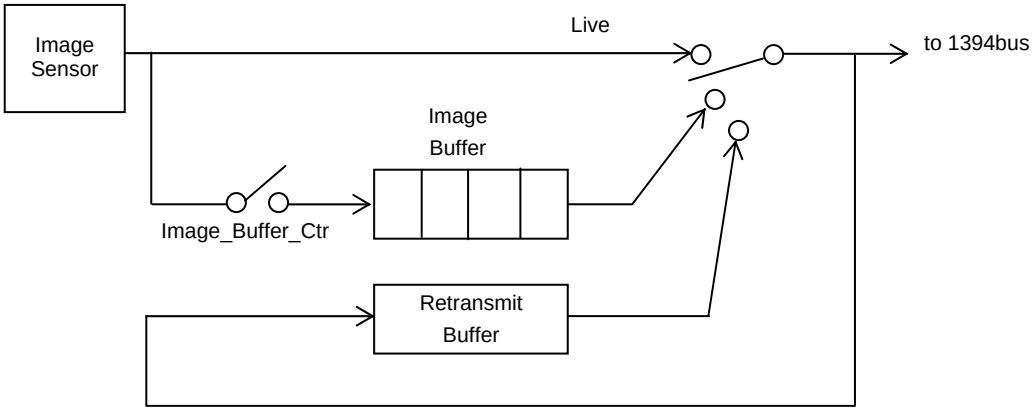
One-Push action:

Camera controls optical filter automatically by itself only once and returns to Manual control state with adjusted value.

A.21 Image Buffer Control

When this function is enabled images are stored in the camera in a circular buffer. Using this function it is possible to transmit from the buffer multiple stored images as well as retransmit the last image transferred. Acquisition and later transmission of stored images is useful when bus bandwidth is limited. Retransmitting an image can be used when reliable image transfer is required.

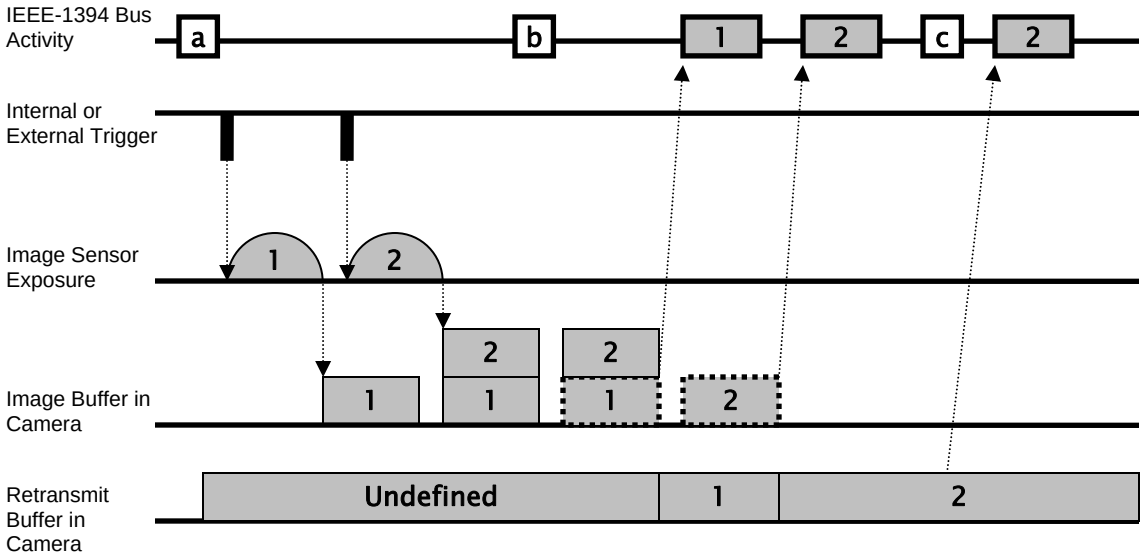
Note that a camera may support only image buffer read, or only image retransmit or both as described by the Image_Buffer_Inq and Retransmit_Inq bits.



Data to be transmitted by ISO_EN, Transfer_data_select, One_Shot and Multi_Shot

ISO_EN/ Continuous_Shot	Transfer_Data_Select	One_Shot/ Retransmit	Multi_Shot/ Image_Buffer_Read	Data to be transmitted
'1'	'X' (Don't care)	'X'	'X'	Live data - Continuous
'0'	'0' (Live data)	'1'	'X'	Live data - One_shot
		'0'	'1'	Live data - Multi_shot
	'1' (Buffered data)	'1'	'X'	Buffered data - Retransmit Buffer
		'0'	'1'	Buffered data - Image Buffer

In the example shown in the figure below, transaction "**a**'' is a write request to register Image_Buffer_Ctr enabling the image buffer function. Subsequently two images are acquired and stored in the camera. Transaction "**b**" is a write request to the Multi_Shot bit with Count_Number set to two and Transfer_Data_Select set to one. The camera then isochronously transfers the two images on the bus from its buffer. Transaction "**c**" is a write request to the One_Shot bit. The camera then retransmits the last image.



Annex B
(informative)

Unit of Value for Absolute Value Control

The following tables describe unit of the value for absolute value control for each feature element.

Meaning of Value type:

Absolute: Value is absolute value.

Relative: Value is absolute value but reference point is system dependent.

B.1 Feature elements High

Feature element name	Function	Unit	Reference point	Value type
Brightness	Black level offset	%	----	Absolute
Auto Exposure	Auto Exposure	EV	0	Relative
White Balance	White Balance	K	----	Absolute
Hue	Hue	deg	0	Relative
Saturation	Saturation	%	100	Relative
Shutter	Integration time	s	----	Absolute
Gain	Circuit gain	dB	0	Relative
Iris	Iris	F	----	Absolute
Focus	Focus	m	----	Absolute
Temperature	Temperature	K	----	Absolute
Trigger	External Trigger	times	----	Absolute
Trigger Delay	Internal Trigger Delay	s	----	Absolute
Frame_Rate	Frame rate	fps	----	Absolute

Definitions for other feature elements, which are not listed above, will be defined in the future.

B.2 Feature elements Low

Feature element	Function	Unit	Reference point	Type
Zoom	Zoom	power	1 (Wide end)	Relative
Pan	Pan	deg	0	Relative
Tilt	Tilt	deg	0	Relative

Definitions for other feature elements, which are not listed above, will be defined in the future.

EV: exposure value

K: Kelvin

deg: degree

s: second

dB: decibel

F: F number

m: meter

fps: frame per second

For the feature of "Hue", + means counterclockwise, - means clockwise on the vector scope.

For the feature of "Pan", + means turning to clockwise, - means turning to counterclockwise.

For the feature of "Tilt", + means turning to upward, - means turning to downward.

Annex C
(normative)

Functional Conformance Test

This section indicates minimum required functional conformance test procedure for the IIDC v1.3x camera and shows the check sheet example.

C.1 Test Procedure

Test 1. Read Configuration ROM

Process: *Requester device (PC) reads the configuration ROM of Responder device (Camera).*

Check Point: *Check the listed values are same as the Responder's defined value.*

Test 2. Read Current Camera Status

Process: *Requester device reads status register of camera*

Check Point: *Check current camera status for video format/mode/frame and ISO transfer status.*

Test 3. Read Inquiry Register for Format/Mode/Frame Rate

Process: *Requester device reads inquiry register of camera*

Check Point: *Check current camera implementing state for current video format/mode/frame.*

Test 4. Read Feature Element Register

Process: *Requester device reads inquiry feature element register of camera*

Check Point: *Check current camera status for each implemented feature.*

Test 5. Control Features

Process: *Requester device controls each feature of camera*

Check Point: *Check current camera status for each controlled feature.*

Test 6. Read Image Transfer Format (Only format_7)

***Process**:* *Requester device reads CSR for format_7*

***Check Point**:* *Check current image transfer format and transfer parameter of the camera.*

Test 7. Isochronous Data Transfer

***Process**:* *Requester sets isochronous image data transfer bit and get image data from the camera.*

***Check Point**:* *Check isochronous data transfer sequence and received data reasonability*

C.2 Check Sheet Example

Attached IIDC functional conformances check sheets covers minimum requirement; this includes device compatibility of IIDC v.1.3x compliant device and ability of control, image capturing and so on.

The testers do these tests according to the check sheet and write the result as followings.

Mark	*Meaning*	*Description*
P	*Pass*	*Test is complete without problem.*
F	*Fail*	*Test cannot be completed with some problem. In this case, the problems should be written in the space of "Remark".*
NA	*Not available*	*Test cannot be done since the function is not available.*

IIDC v1.3X Functional Conformance Test Check Sheet

Test Date	/ / (D/M/Y)
Tester	
Tested Equipments	

Test 1	Read Configuration ROM						
		R/W	Address	Expected Value	Check Point	Result	Remarks
	Rom CRC value	RD	Bus info 400h/16...31	Calculated value	Value is correct		
	Node vender ID	RD	Bus info 40Ch	SD( )	Value is correct		
	Chip ID	RD	Bus info 40C,410h	SD( )	Value is correct		
	Max rec	RD	Bus info 408h	SD( )	Value is correct		
	CRC of Root Directory	RD	Root Directory 414h/16...31	Calculated value	Value is correct		
	CRC of Node unique ID	RD	Node unique ID+0h/16...31	Calculated value	Value is correct		When the target device depend on 1394-1995
	CRC of Unit Directory	RD	Unit directory+0h/16...31	Calculated value	Value is correct		
	Unit spec ID	RD	Unit directory(Key=12h) /8...31	0A02Dh	Value is correct		
	Unit SW version	RD	Unit directory(Key=13h) /8...31	000102h	Value is correct		
	CRC of Unit dependent	RD	Unit dependent+0h/16...31	Calculated value	Value is correct		
	Command register base	RD	Unit dependent+004h/8...31	SD( )	Value is correct		
	CRC of Vender name	RD	Vendor name+0h/16...31	Calculated value	Value is correct		
	Vendor name	RD	Vendor name leaf + 00Ch	SD( )	Value is correct		
	CRC of Model name	RD	Model name+0h/16...31	Calculated value	Value is correct		
	Model name	RD	Module name leaf +00Ch	SD( )	Value is correct		
	Unit sub sw version	RD	Unit dependent+0010h/8..31	000010h	Value is correct		

Test 2	Read default camera status						
		R/W	Addrress/Bit position	Expected value	Check Point	Result	Remarks
	Current video format	RD	Base+608h/0..2	SD( )	Value is correct		
	Current video mode	RD	Base+604h/0..2	SD( )	Value is correct		
	Current video frame rate	RD	Base+600h/0..2	SD( )	Value is correct		Except Format7
	ISO_channel	RD	Base+60Ch/0..3	SD( )	Value is correct		For legacy mode
	ISO_speed	RD	Base+60Ch/6..7	SD( )	Value is correct		For legacy mode
	ISO_channel_B	RD	Base+60Ch/18..23	SD( )	Value is correct		For 1394.b mode
	ISO_speed_B	RD	Base+60Ch/29..31	SD( )	Value is correct		For 1394.b mode

Test 3	Read Inquiry register for format/mode/frame rate					
		R/W	Addrress/Bit position	Check Point	Result	Remarks
	Video format	RD	Base+100h/0..7	The bit which corresponding Current Format must be 1		
	Video Mode	RD	Base+180h - 19Ch	The bit which corresponding Current Mode must be 1		
	Frame Rate	RD	Base+200h - 25Ch	The bit which corresponding Current Frame Rate must be 1		Except Format7
	Format7 offset address	RD	Base+2E0h - 2FCh	Value is correct		Offset address for Format7 CSR

Test 4	Read feature element						
		R/W	Address/Bit position	Expected value	Check Point	Result	Remarks
	Basic Function	RD	Base+400h	SD( )	Value is correct		
	Feature Presence	RD	Base+404h, 408h	SD( )	Value is correct		
	Opt Function Presence	RD	Base+40Ch	SD( )	Value is correct		Only when this function is available (When the bit of Basic_Function[3] is 1)
	Advanced Feature offset	RD	Base+480h	SD( )	Value is correct		Only when advanced feature is supported. (When the bit of Basic_Function[0] is 1)
	PIO Control offset	RD	Base+484h	SD( )	Value is correct		Only when this function is available (When the bit of Opt Function_Presence[1] is 1)
	SIO Control CSR	RD	Base+488h	SD( )	Value is correct		Only when this function is available. (When the bit of Opt Function Presence[2] is 1)
	Strove Output CSR	RD	Base+48Ch	SD( )	Value is correct		Only when this function is available. (When the bit of Opt Function Presence[3] is 1)
	Feature Element	RD	Base+500h - 5C4h	SD( )	Value is correct		

Test 5	Control features					
		R/W	Address/Bit position	Check Point	Result	Remarks
	each feature CSR	WR/RD	Base+800h - 88Ch	Controlled status is correct		
	Absolute value	WR/RD	Base+700h - 78Ch	Value is correct		Only for supported feature.
	Control Status	RD	Base+640h-644h	Value is correct		

Test 6	Read image format		(Only format_7 Camera)				
		R/W	Address/Bit position	Expected value	Check Point	Result	Remarks
	Image size (Horizontal)	RD	CSR+00Ch/0..15	SD( )	Value is correct		
	Image size (Vertical)	RD	CSR+00Ch/16..31	SD( )	Value is correct		
	Color cording	RD	CSR+010h/0..7	SD( )	Value is correct		
	Total byte	RD	CSR+038h,03Ch	SD( )	Value is correct		
	Rec_Byte_Per_Packet	RD	CSR+044h/16..31	SD( )	Value is correct		
	Packet_Per_Frame	RD	CSR+048h/0..31	SD( )	Value is correct		

Test 7	Image data transfer		(At factory default mode)			
		R/W	Address/Bit position/Data	Check Point	Result	Remarks
	Byte_Per_Packet	WR	Format7CSR+044h/0..15	Write value is recommended correctly		Only Format_7
	Operation mode	RD	Base+60Ch/16	Current value is correct		
	ISO channel	RD	Base+60Ch/0...3	Current value is correct		For legacy mode
	ISO Speed	RD	Base+60Ch/6...7	Current value is correct		For legacy mode
	ISO channel	RD	Base+60Ch/18...23	Current value is correct		For 1394.b mode
	ISO Speed	RD	Base+60Ch/29...31	Current value is correct		For 1394.b mode
	Start ISO Transfer	WR	Base+614h/0/1	ISO transfer is started		
	Image data			Display image is correct		
	Stop ISO Transfer	WR	Base+614h/0/0	ISO transfer is stopped		

P: Pass F: Fail NA: Not Available
SD: System Dependent

Annex Table C-1 Check Sheet

Annex D
(informative)

Bibliography

[D1] IEEE Std 1212-2001, Standard for a Control and Status Registers (CSR) Architecture for microcomputer buses

[D2] IEEE Std 1394-2008, Standard for a High Performance Serial Bus

[D3] ISO/IEC 9899:1990, Programming Languages—C